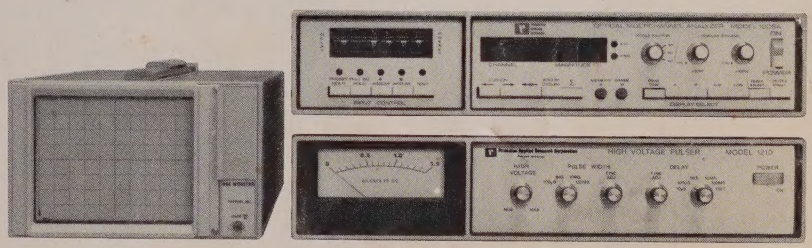
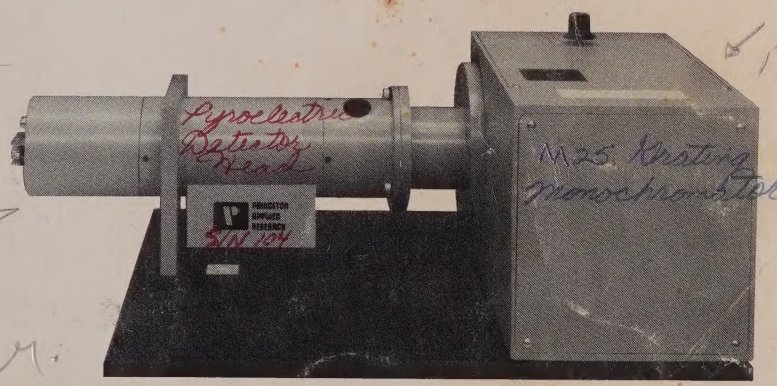
MODEL 1205A

OPTICAL MULTICHANNEL ANALYZER OMA®

TEXTRONIX 604 MONITOR



MODEL 1204A Flat 3-10 μ. slight roll off ~ 12 μ. ½ wide det. array



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OPERATING AND SERVICE MANUAL

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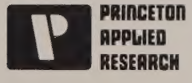
PRINCETON APPLIED RESEARCH

OPTICAL MULTICHANNEL ANALYZER OMA®

OPERATING AND SERVICE MANUAL



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OPTICAL MULTICHANNEL ANALYZER SYSTEMS

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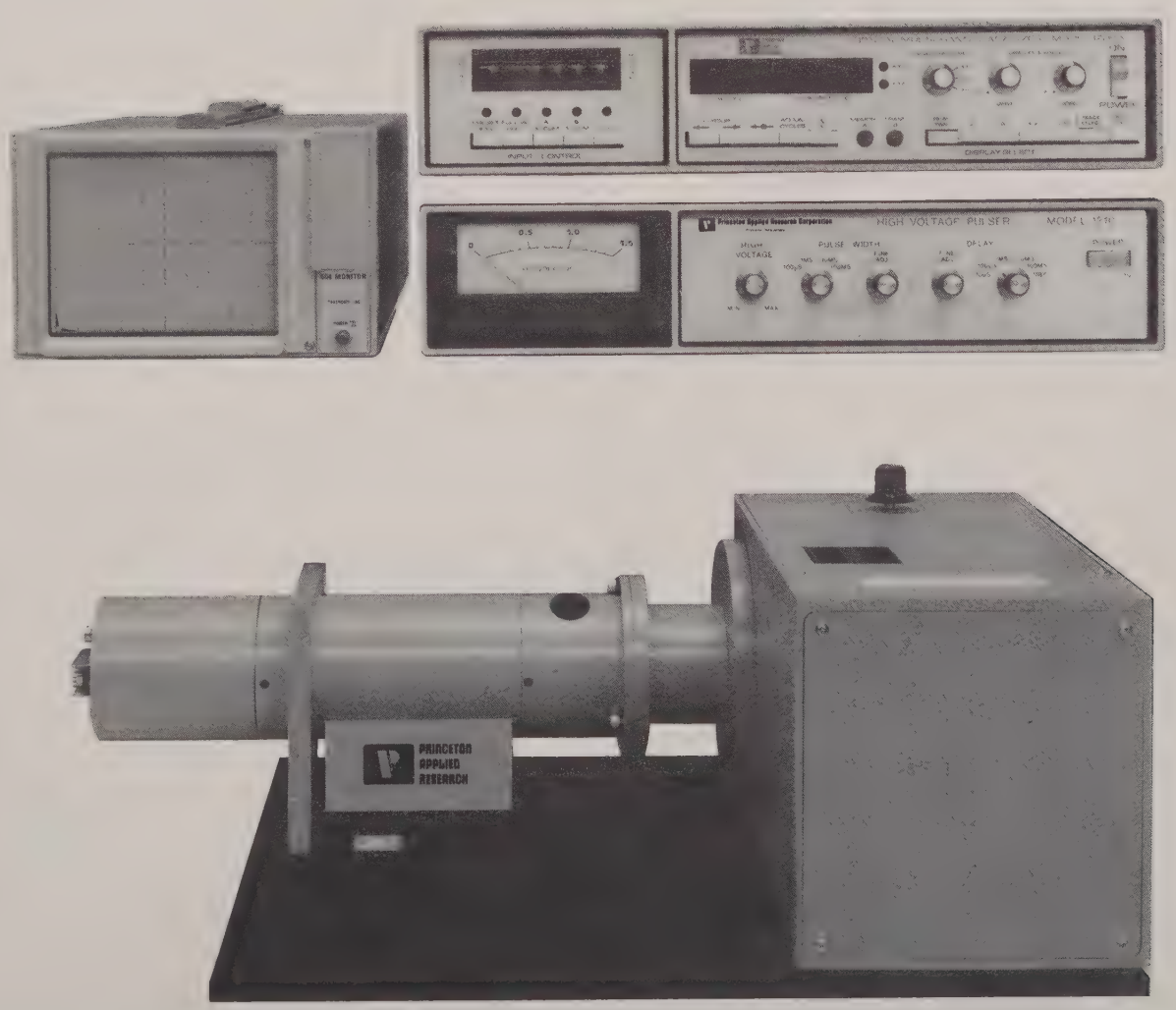


THE GATED OPTICAL MULTICHANNEL ANALYZER SYSTEM SHOWN INCLUDES A POLYCHROMATOR (1208), MONITOR SCOPE (604), CONSOLE (1205A), 1205D SILICON INTENSIFIED TARGET DETECTOR (SIT) AND 1210 GATE PULSE GENERATOR. GATING IS ELECTRONIC SHUTTERING FOR FINE TIME RESOLUTION.

SECTION I
CHARACTERISTICS

1.1 DESCRIPTION

The 1200 Series is a family of instruments designed for the simultaneous measurement of light in a linear array of 500 channels. In Figure I-1, a spectrum is shown dispersed across the 500 channels of the standard 1205B Detector. The signal from the Detector is digitized by the 1205A Console, stored in a solid state memory, and is used to refresh the display on an X-Y display scope. The front panel digital display gives the digital contents of the memory for any channel. The spectrum being displayed was recorded in 32.8 ms.

The detectors used for the OMA have three characteristics in common. First, they are all storage devices, i.e., all 500 channels are active simultaneously. Second, they are linear with respect to light intensity (if the light intensity doubles, the signal from the detector doubles). Third, the detectors are read one channel at a time by a scanning electron beam.

The detector housing also contains a low-noise, controlled-bandwidth preamplifier. The high level signal from this preamplifier is routed to the 1205A Console for further processing.

The console has several functions. The first of these is to digitize the signal from the detector. Once in digital form, the data may be directed to either of two 500-word, 21-bit memories (Memory A and Memory B). These memories may be used to store the result of a single 32.8 ms (one frame) exposure or to signal-average many exposures, thus improving both the signal-to-noise ratio and the dynamic range. Signal-to-noise improvements of more than 100 times that of a single scan are easily attained. Generally, the A memory is used to store the desired signal plus undesired signals (such as stray light and detector dark current) and the B memory is used to store the undesired signals alone. The two memories may then be subtracted channel-by-channel to yield the desired signal. Once the data is in this form, each channel may be read digitally on the front panel or may be directed to a printer or computer from a back-panel connector. A high-speed analog output is used to drive an X-Y display scope, and a slow analog output is available for plotters.

1.2 OPERATING MODES

1.2A INPUT MODES

In every input mode, the data from all five hundred detector channels is read into a memory. The data may be added (accumulated) to the A memory (A ACCUM), to the B memory (B ACCUM), or to both for any number of scans. It is also possible to select a delay of from zero-to-eleven times 32.8 ms between active read-in cycles. This allows the signal to accumulate on the detector before being applied to the preamplifier, thus improving the signal-to-noise ratio for weak signals. In addition, there is a test mode which provides a test input level (usually set to deliver 100 counts to each channel every read-in cycle) with an artificial peak after the cursor channel.

Accumulations may be automatically stopped in two ways. Selecting the full scale hold (FULL SC HOLD) mode will stop the accumulation when the count in any channel reaches or exceeds 98,000. Selecting the preset hold (PRESET HOLD) mode will cause the accumulation to stop after a preset number of read-in cycles. The accumulation time will be the number set on the PRESET switch (P), times the DELAY (D) switch setting plus one, times 32.8 ms, or 32.8 (P) (D+1) ms (see Subsection 4.6B). The measurement may be manually stopped at any time by releasing the ACCUM buttons.

To make a measurement, the operator would normally: (a) select FULL SC HOLD or PRESET HOLD, (b) select a PRESET count and DELAY (from zero to eleven), (c) erase the A memory, and (d) push A ACCUM button. When the accumulation is complete, the light over the ACCUM A button will go out and the light over the FULL SCALE or PRESET HOLD button will come on. The ACCUM A button should then be released.

For longer delays with cooled vidicons, the functions of the PRESET and the DELAY digital switches may be reversed by internal switches. For very long delays with 1205K series detectors at dry ice temperatures, the 1207 Extended Delay Accessory may be attached to the 1205.

1.2B DISPLAY MODES

The output of either memory ("A" or "B"), the channel-by-channel difference ("A–B"), or the REAL TIME (single frame scans of the vidicon) may be displayed on an X-Y display scope. There are two controls to select the vertical sensitivity for the scope; the SCALE FACTOR switch selects the magnitude of the most significant digit read from the memory to the display D-A converter. The VERTICAL EXPAND control varies the vertical gain from X1 to X10. There is also a log display mode in which the log of the selected data source is displayed (this mode of presentation approximates a true log to ±3% and provides linear interpolation between logarithmic decades).

An intensified channel on the display marks the location of the cursor. The cursor channel number is read out digitally on the front panel. The contents of this channel are also read out digitally and identified as MAGNITUDE. The source of the digital data will be the same as for the display data. The cursor may be moved to the right (increasing channel number) by pushing the button marked "→", or to the left (decreasing channel number) by pressing "←" or returned to channel zero by pressing "⇤0⇥".

The display may be expanded in the horizontal direction by turning the HORIZONTAL EXPAND control. In this mode, the display starts expanding at a point twelve channels to the left of the cursor.

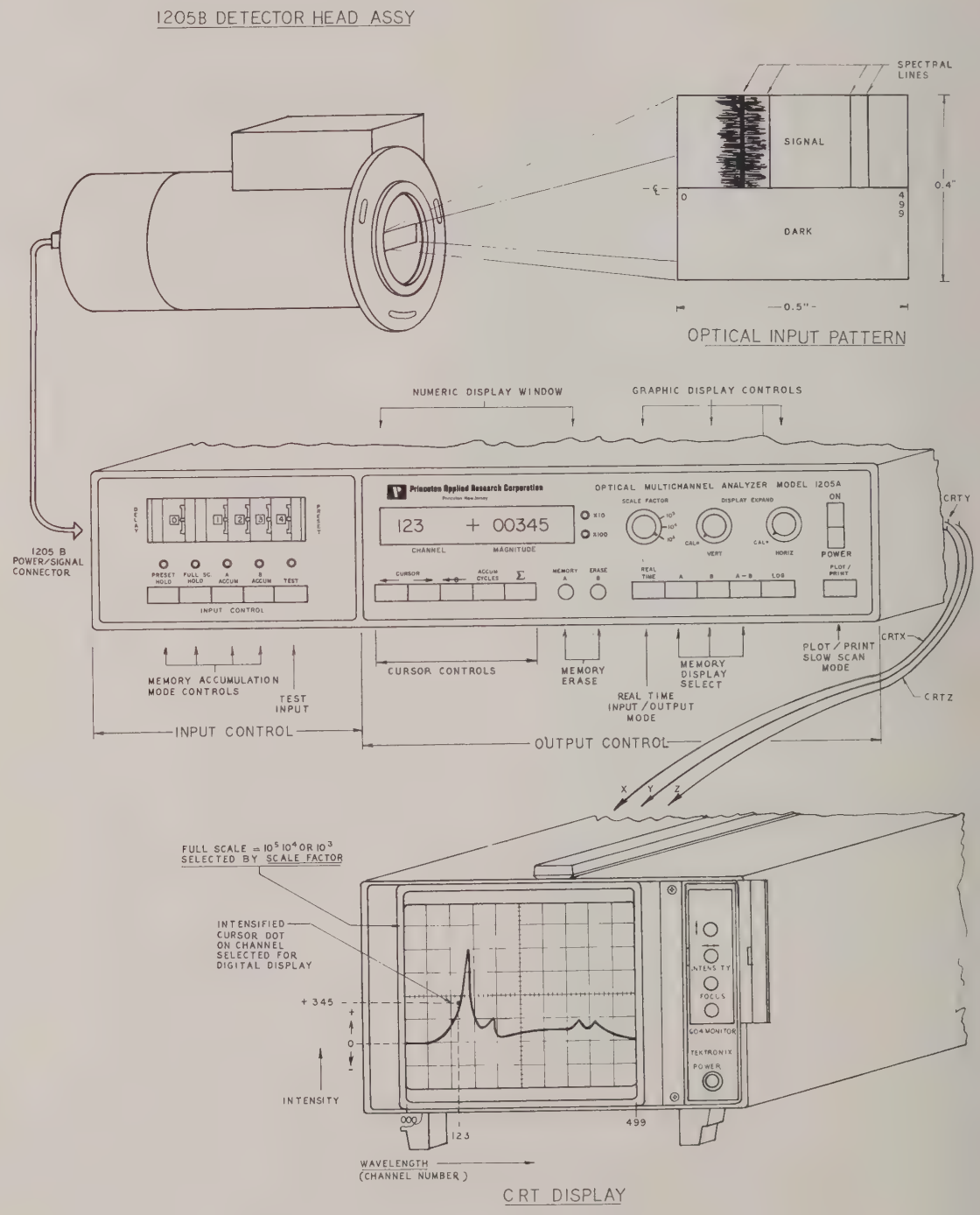


Figure I-1. OPTICAL MULTICHANNEL ANALYZER IN TYPICAL APPLICATION

When the ACCUM CYCLES pushbutton is pushed, the digital readout will display the number of 32.8 ms periods during which data was accumulated in the selected display source (for "A–B" the difference in the number of accumulation cycles is presented).

The Σ button selects a summation mode. In this mode it is possible to sum the contents of any number of adjacent channels. This is done by positioning the cursor on the leftmost channel to be summed and then pushing the Σ button. The cursor is then moved to the right until it is over the rightmost channel to be summed. The summation will appear at the digital display. Moving the cursor from right-to-left will subtract the contents of each channel from the summation. The displayed sum is multiplied by X10 or X100 as selected by a switch on the back panel and indicated by an LED to the right of the display.

1.2C OUTPUT MODES

The standard 1205A provides outputs suitable for driving an X-Y plotter, a point plotter, or a printer. The PLOT/PRINT mode is selected to drive one of these devices. In this mode, the PLOT RATE control on the back panel becomes active and controls the rate at which the channels are read out. This rate is variable from 32.8 ms per channel ("1") to 11 x 32.8 ms per channel ("11"). When set to "0", the readout device must provide an advance signal. This position would be used for point plotters or for a parallel printer. Without selecting the PLOT/PRINT mode, it is still possible for a computer or other device to interrogate the 1205A for the contents of any or all channels. The control lines for this function are on the back panel and are TTL compatible. See Section IX.

1.2D REMOTE PROGRAM CAPABILITY

All functions of the Optical Multichannel Analyzer (except for analog display expansion) may be remotely operated via the TTL inputs and outputs on the rear panel of the instrument.

1.3 SPECIFICATIONS

1.3A 1205A OMA CONSOLE

Useful dynamic range from memory: 10^4 (80 dB)
Useful dynamic range, analog output: 10^3 (60 dB)
Useful dynamic range, real time: 7.5×10^2 (57 dB)
Memory count range: 10^5 counts per channel
Number of active channels per memory: 500
Number of memories: 2
Frame scan time: 32.768 ms
Line scan time: 64 μs
Maximum integration time per input cycle: 12 x 32.768 ms = 0.393 s
Number of preset input cycles: 1×10^4
Digital output levels: TTL
Digital data output format: 5 BCD digits + sign
Digital output identification: 3 BCD digits for channel number + coded (4 wires) source
Digital input: all front panel controls (except analog display controls), parallel channel numbers, data request, and ready
Input overload indication: 732/scan in any CHANNEL
Linear overrange: 783/scan (+7%) in REAL TIME; 860/scan (+17%) in ACCUM modes.

1.3B 1205B, E, F, or G WITH 1205A

Sensitivity: see graphs
Geometric linearity: ±2 channels straight line reference
Uniformity of sensitivity: ±10%; ±4% for an integrated peak
Reproducibility of sensitivity: ±0.5%
Resolution: 20 line pairs per mm at 50% MTF
Operating temperature range: −10°C to 35°C
Crosstalk: with a 10 μm line centered on Channel N, >60% of signal will be in Channel N, >98% of signal will be in Channels N−1, N, and N+1
Linearity as function of intensity: ±1% for 10 to 500 counts per frame
Useful delay at 25°C: 3 x 32.768 ms = 98 ms

1.3C 1205D WITH 1205A

Sensitivity: see graphs
Geometric linearity: ±4 channels straight line reference
Uniformity of sensitivity: ±20%; ±10% for an integrated peak
Reproducibility of sensitivity: ±1%
Resolution: 15 line pairs per mm at 50% MTF
Operating temperature range: −10°C to +35°C
Crosstalk: with 10 μm line centered on Channel N, >50% of signal will be in Channel N, >97% of signal will be in Channels N−1, N, and N+1
Linearity as function of intensity: ±1% for 10 to 500 counts
Useful delay at 25°C: 3 x 32.768 ms = 98 ms

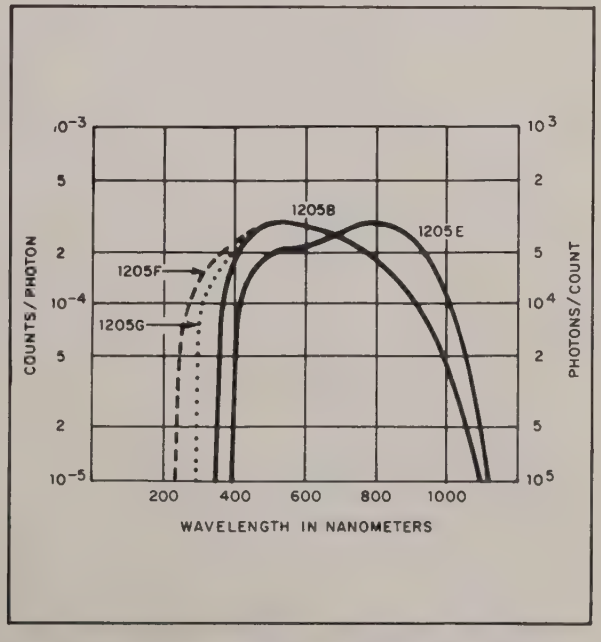


Figure I-2. RESPONSE vs WAVELENGTH FOR 1205B, E, F, & G

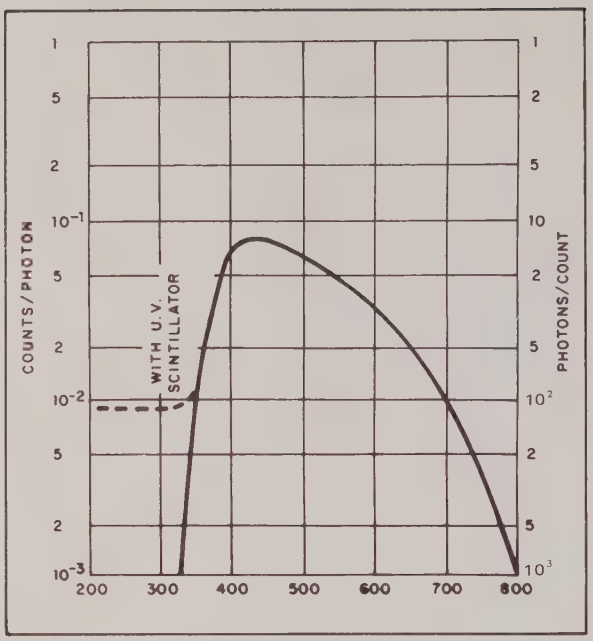


Figure I-3. RESPONSE vs WAVELENGTH FOR 1205D

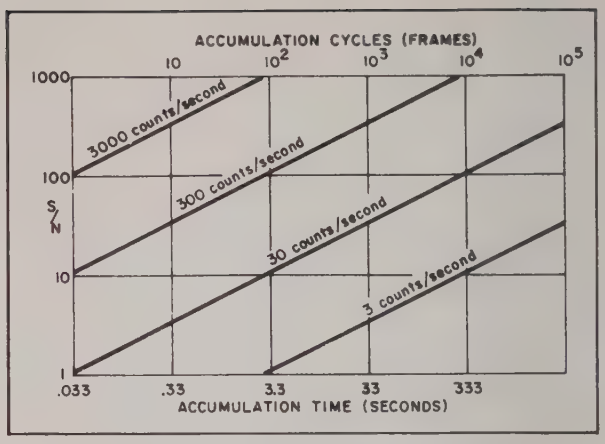


Figure I-4. SIGNAL-TO-NOISE RATIO vs TIME FOR 1205B, E, F, AND G

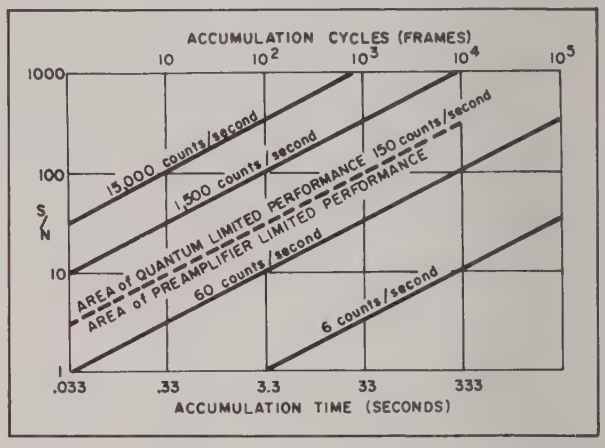


Figure I-5. SIGNAL-TO-NOISE RATIO vs TIME FOR 1205D

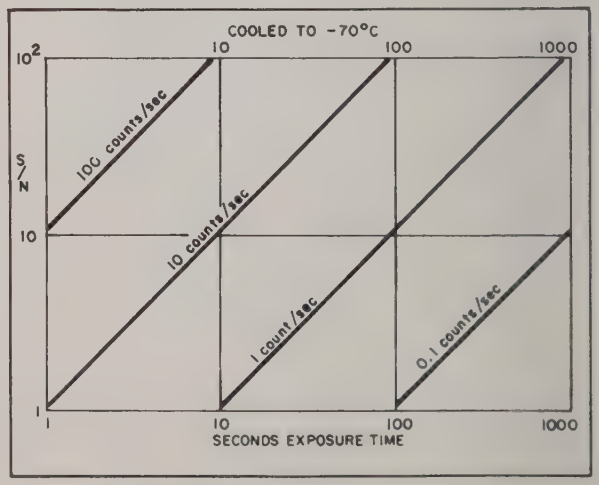


Figure I-6. SIGNAL-TO-NOISE RATIO vs TIME FOR 1205KB, KE, KF, & KG

1.3D FRONT-PANEL CONTROLS 1205A OMA CONSOLE

ACCUMULATE MODE SELECTION
- Accumulate to A Memory
- Accumulate to B Memory
- Preset Hold
- Full-Scale Hold
- Test

ACCUMULATION TIME SELECTION
- Number of Delay Frame Times per Input Cycle
- Number of Preset Input Cycles

MEMORY ERASE CONTROLS
- Erase A Memory
- Erase B Memory

DISPLAY MODE SELECTION
- A Memory Only
- B Memory Only
- A Minus B
- Real Time
- Log of Any of the Above (Analog Only)
- Print/Plot (Output of Any Above)

DISPLAY CONTROLS
- Analog Scale Factors (10^5, 10^4, or 10^3 Counts Full Scale)
- Vertical Expand
- Horizontal Expand

SINGLE CHANNEL DIGITAL READOUT SELECTION
- Cursor Left
- Cursor Right

Cursor Zero
A Memory Readout
B Memory Readout
A Minus B Readout
Accumulation Cycles Readout
Summation Readout

PRIMARY POWER
On-Off (with Pilot Light)

1.3E REAR-PANEL CONTROLS, INPUTS AND OUTPUTS: 1205A OMA CONSOLE

CONTROLS
Plot/Print Rate (32.8 - 350 ms per Channel)
110/220 Input ac Voltage Selection
Summation X10 or X100

INPUTS
110/220 V Primary Power
Detector Head Preamp Signal (on Multi-Pin Connector)
TTL Remote Program

OUTPUTS
CRT X Axis Drive (0 to 1.5 V fs, Adjustable)
CRT Y Axis Drive (−.8 V to +.8 V fs, Adjustable)
CRT Z Axis Drive (+1 V to −1 V, Adjustable)
Plotter Y Axis Drive (−1 V to +1 V fs, Adjustable)
Plotter X Axis Drive (0 to 1 V, Adjustable)
Single Channel Marker/Cursor
Real Time Video
TTL Digital Outputs for Printer or Computer
Vidicon Power and Control Signals (on Multi-Pin Connector)

POWER INPUT
110/220 V ±10%, 50-60 Hz
80 watts

DIMENSIONS
1205B, E, F, and G Detector Heads: 9.5" x 4.5" x 3.2" (24 cm x 11.6 cm x 8.1 cm)
1205A Console: 17" x 15.5" x 3.5" (W.D.H.); (43 cm x 39 cm x 8.9 cm)
1205D Detector Head: 12.7" x 4.5" x 3.2" (32 cm x 11.4 cm x 8.1 cm)
1205B, KE, KF, and KG: 13.25" x 10.25" x 11.75" (34 cm x 26 cm x 30 cm)

WEIGHT
1205A Console: 20 lb (9.1 kg)
1205B, E, F, & G Sensor Head: 5 lb (2.3 kg)
1205D Sensor Head: 6½ lb (3 kg)

1.4 CONSTRUCTION

The Model 1205A Optical Multichannel Analyzer Console is contained in an enclosure similar to that of other Princeton Applied Research Corporation* instruments. It employs a cast aluminum front-panel bezel, steel side panels, aluminum rear panel to accommodate options, inner steel chassis, a slip over cover, and a bottom plate with flip-up stand. The power supply is contained on one printed circuit board and all logic boards plug into an interconnecting mother board.

The Detector Head Assembly is a separate unit housing the vidicon detector, the deflection coils, and the low noise preamplifier. The standard 1205B, E, F, or G housing is a machined aluminum enclosure consisting of a cylindrical section with mounting flange containing the vidicon and coils, and an integral separately-shielded box for the preamplifier.

1.5 OPTIONS

Refer to Section V of this manual for a complete discussion of options. These include the following.

Model 1205A Console
-03 Option: Serial Converter
-05 Option: Dual Head Card Set
-06 Option: Magnetic Tape Controller
-07 Option: Interface Autocycle Mode Printer Option for H.P. Digital Printer 5055A-H49.
-08 Option: Two Dimensional OMA

Detector Head
1205B: Standard Si Vidicon Detector
1205D: Intensified Detector (16 mm)
1205E: IR Enhanced Vidicon Detector
1205F: UV Enhanced Vidicon Detector
1205G: Quartz Si Vidicon Detector Head
1205K Dry Ice Cooled Housing

*Referred to hereafter as P.A.R.C.

SECTION II
INSTALLATION

2.1 UNPACKING AND INSPECTION

This instrument was thoroughly tested and inspected before shipment and should be ready for use when received.

After the instrument is unpacked, it should be inspected carefully for any damage received in transit. If any shipping damage is found, the carrier should be notified as soon as possible. Save the shipping container for inspection by the carrier.

2.2 LOCATION AND MOUNTING — MODEL 1205A O.M.A. CONSOLE

The OMA console is designed for bench operation or rack mounting (brackets are included). It can be placed in any desired location. However, locations where chemicals or corrosive agents may be splashed or sprayed on the instrument should be avoided.

CAUTION

Do not place instrument on or near heat generating equipment that may cause ambient temperature to rise above 35°C. This instrument does generate heat and will require forced air cooling if placed in a restricted air flow environment.

2.3 LOCATION AND MOUNTING — DETECTOR ASSEMBLY

2.3A INTRODUCTION

The Model 1205B Detector Assembly and optional units are designed for mounting directly to any P.A.R.C. spectrometer or, through the use of an adapter plate, to most other commercially available instruments. Three mounting through-holes are provided, equally spaced on a 3.600" diameter circle. These holes are 0.20" diameter slots allowing a ±10° alignment rotation (see Figure II-1). The scan pattern on the face of the vidicon uses an area of 0.5 x 0.4 inches. This area is divided into two equal parts and the dispersed portion of a spectrum should be focused on the lower half of this area. See Section IV, Subsection 4.5, for alignment and focusing instructions.

2.3B GENERAL PRECAUTIONS

(1) Detector Damage

The Vidicon Detector faceplate, which is accessible at the front of the unmounted Detector Assembly, is quite fragile. A cap is provided to protect the Vidicon Detector faceplate against damage from fingerprints and dirt.

(2) Intensifier Damage

Intensifier Detector Assemblies (1205D, etc.) may

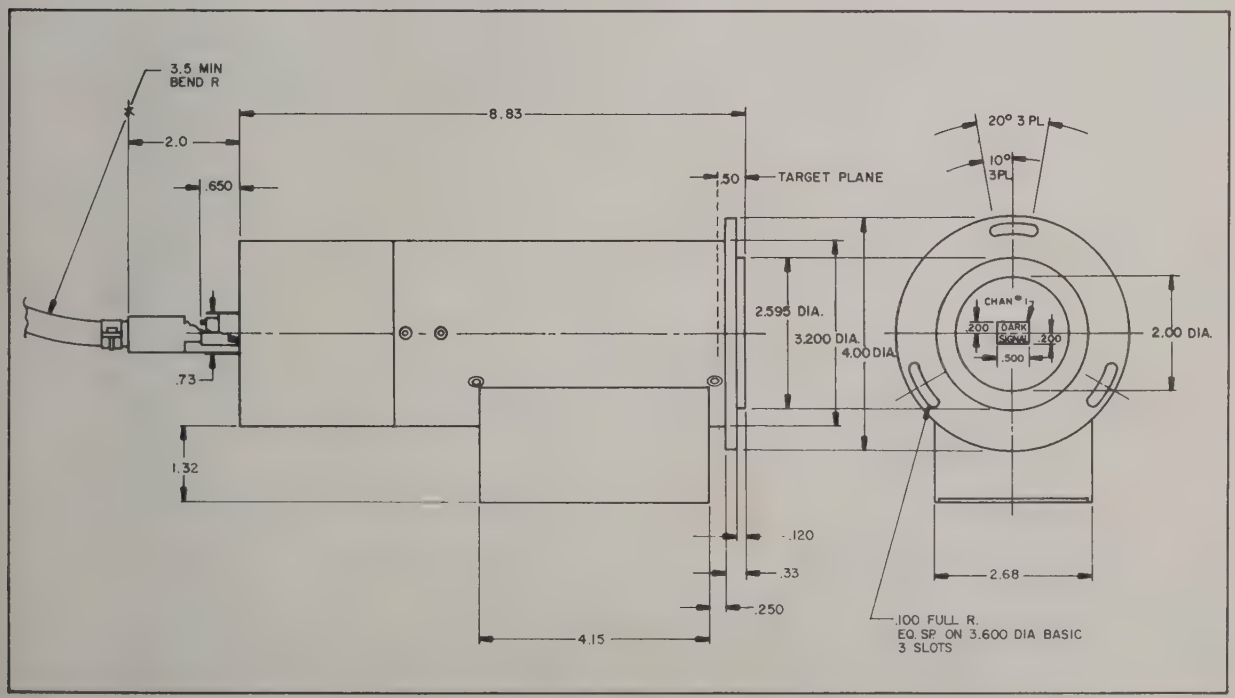


Figure II-1. DETECTOR ASSEMBLY OUTLINE DRAWING (1205B, E, F, and G)

suffer major damage as a result of excessive light input. The safety precaution listed in the application notes for these detectors must be observed before connecting or applying power to an Intensifier Detector Assembly. In general, this detector should be treated as carefully as a photomultiplier.

(3) High Voltage

HIGH VOLTAGES ARE PRESENT on some pins of the 1205A/B POWER/SIGNAL connectors, and within the 1205A and Detector.

To allow these voltages to bleed off, the power must be OFF for at least *one minute* before connecting or disconnecting either end of the power/signal cable.

CAUTION

The four coaxial cable connector pins on the power/signal cable may be damaged by the use of excessive force in connecting the cable at either end. If all of the pins are aligned, little force is required. Pin alignment is facilitated by using a slight vertical and horizontal rocking motion of the cable plug when making the connection. The outer "ears" on the plugs should be bent inwards during insertion so as to achieve mechanical locking after the plug is attached.

(4) Connector Damage

Do not stand the Detector Assembly on its connector end, as this will damage the subminiature pin (pin #2). This pin extends beyond the rest of the other pins in the connector. If any pin can be pushed into the connector block by light finger pressure, either the connector block or the retaining clip has been damaged.

(5) Magnetic Fields

Operation of the Detector Assembly in the presence of magnetic fields should be avoided.

(6) Other Detector Assemblies

Optional Detector Assemblies (intensifier, cooled, UV, etc.) are discussed in Section V - OPTIONS AND ACCESSORIES, or in special application notes or manuals. See your local P.A.R.C. representative for current options information.

2.4 LINE VOLTAGE AND POWER REQUIREMENTS

This instrument may be used on either 115 V ac or 230 V ac, 50-60 Hz. The appropriate voltage may be selected by a rear-panel switch. The instrument is normally shipped with the SELECTOR SWITCH in the 115 V position for domestic customers and in the 230 V position for overseas customers. Power consumption is typically 80 watts.

2.5 PERFORMANCE CHECK

Before the line cord is plugged in, please check to see that the AC SELECTOR switch (rear panel) is in the proper position (115 or 230). The line cord may now be inserted and the following tests made. These tests do not require the connection of the Detector Assembly. The tests should be performed in sequence, as each depends upon previous settings and results.

2.5A SETUP

Set the controls on the 1205A OMA console as follows.

Rear Panel
PLOT RATE: 9
X10-X100 toggle switch: X10

Front Panel
DELAY: 0
PRESET: ØØ1Ø
TEST pushbutton: set
"A" SELECT DISPLAY: set
remaining pushbuttons: released

2.5B POWER ON

Push the POWER rocker arm switch to ON and observe that:

(1) The neon light in the POWER switch lights.

(2) The TEST status LED lights.

(3) The numeric display window shows all zeros (i.e., CHANNEL number ØØØ MAGNITUDE = ØØØØØ).

2.5C CURSOR

(1) *Momentarily* press the CURSOR UP pushbutton (→). Note that each time this is done, the CHANNEL number in the numeric display window advances to the next higher number.

(2) *Press and hold* the CURSOR UP pushbutton. Note that after a short delay, the CHANNEL number counts continuously upward.

(3) Repeat steps 1 and 2 with the CURSOR DOWN (←) pushbutton. Note that the CHANNEL number counts downward.

(4) Note that at the extremes the CURSOR controls cause the CHANNEL number to count upward from 499 to ØØØ, and downward from ØØØ to 499.

(5) Press the CURSOR ZERO control (→0←) and observe that the CHANNEL number jumps directly to ØØØ.

2.5D MEASUREMENT

(1) Set CHANNEL number 499 by use of the cursor controls.

(2) Press PRESET HOLD (Input Control pushbutton).

(3) Press REAL TIME and record the MAGNITUDE

reading. This is the TEST signal (a non-calibrated number factory set at about +ØØ1ØØ).

(4) Press DISPLAY SELECT pushbutton "A".

(5) Press A ACCUM and note the following sequence:

(a) A ACCUM status indicator lights up.

(b) MAGNITUDE increases in ten steps equal to the TEST signal noted in (3) above.

(c) A ACCUM status lamp is extinguished and PRESET HOLD status lamp lights up.

(d) MAGNITUDE holds at 10 x (TEST signal) ±10. *Note and record this number.*

(6) Release A ACCUM.

(7) Press ACCUM CYCLES and observe:

(a) CHANNEL number is blanked out.

(b) MAGNITUDE = +ØØ1ØØ. +00010

(8) Release ACCUM CYCLES and note return to numeric display as in step 5d.

(9) Press Σ (SUM mode) pushbutton and note:

(a) MAGNITUDE = ØØØØØ.

(b) X10 indicator lit.

(10) Advance the CHANNEL number to ØØØ by pressing the CURSOR UP (→) pushbutton momentarily. Do not use the CURSOR ZERO (→0←) control for this. Note that the MAGNITUDE (including the X10) is 2 x (step 5d MAGNITUDE) ±20.

(11) Using the cursor controls, but *not* CURSOR ZERO (→0←), move the CHANNEL number upwards past Ø1Ø, then downwards past 488, then upward to ØØ7. Note that the MAGNITUDE increases and decreases with the CHANNEL number, and is negative below CHANNEL number 499.

(12) Step the CHANNEL number from ØØ7 up to ØØ8. Note that the MAGNITUDE is now the sum of channels 499 through ØØ8 inclusive, or ten times the single channel reading from step 5d, ±100. (MAGNITUDE = numeric display at the reading noted in step 5d, ±10, and X10 illuminated.)

(13) Using CURSOR DOWN (and not Cursor Zero), step the CHANNEL number downward to 499 and note that the MAGNITUDE = ØØØØØ.

(14) Release the Σ (SUM mode) pushbutton and note a return to the reading of step 5d.

(15) Press MEMORY ERASE A and note that the MAGNITUDE goes to ØØØØØ, and that the PRESET HOLD lamp is extinguished.

(16) Press →0← to set the CHANNEL number to ØØØ.

(17) Press PLOT/PRINT and note the following:

(a) CHANNEL number counts upward.

(b) MAGNITUDE = ØØØØØ for every CHANNEL number (due to memory erase in step 15).

(c) CHANNEL number advance stops automatically when CHANNEL number changes from 499 to ØØØ.

SECTION III
CONTROLS AND CONNECTORS

3.1 GENERAL DESCRIPTION

The basic Optical Multichannel Analyzer system consists of a Detector Head Assembly, the 1205A Console, an accessory CRT (oscilloscope) display unit, and a group of optional output devices. Once the initial set-up has been completed, all OMA functions are operated by use of the front-panel controls on the 1205A Console. The front-panel bezel divides these controls into two major groups, the Input Control group and the Display group.

3.2 INPUT CONTROL GROUP

The Input Control group is at the left of the OMA front panel. This group consists of the DELAY and PRESET thumbwheel switches, and five pushbutton INPUT CONTROL switches. In an OMA measurement sequence, the input control group controls the measurement time and duration, and the transfer of input signal information from the Detector Head to one or both of the OMA memories. A TEST input mode is also provided.

3.2A DELAY SWITCH

The single-digit DELAY thumbwheel switch selects the number (from 0 to 11) of the delay cycles in each input cycle. A delay cycle is one accumulation cycle (32.768 ms) of extra signal integration time before the vidicon is scanned. If a DELAY of 2 were selected, a delay time of 2 x 32.768 ms (65.536 ms) would occur before each active scan cycle, and each input cycle would add three accumulation cycles (or 98.304 ms) of integrated light signal into the memory. The maximum usable setting of this control depends on the input signal level, on the vidicon dark current, and on the temperature. At room temperature (25°C), the maximum usable setting is typically 3 or 4.

3.2B PRESET SWITCH

The four-digit PRESET thumbwheel switch selects the number of input cycles that will occur before a measurement is automatically stopped in the PRESET HOLD mode. Each input cycle is made up of delay cycles and an active scan cycle, and may be one or more accumulation cycle times in duration. See Table III-1 for the relationship between desired accumulation time and actual accumulation time as a function of different numbers of complete accumulation cycles.

3.2C PRESET HOLD

When the PRESET HOLD button is depressed, a measurement will stop automatically after the number of input cycles set on the PRESET switch has been added to the memory. When this number has been reached, the light above the button will come on. The preset counter is reset by releasing this button or by erasing either memory.

3.2D FULL-SCALE HOLD

With the FULL SC HOLD button depressed, the accumulation time is determined by the number of counts in the memory. An accumulation will be terminated when any channel reaches a number greater than +98,000. When the number of counts in any channel in the selected memory exceeds +98,000, the light above this button will come on whether the button is depressed or not.

3.2E A ACCUM

When the A ACCUM button is depressed, counts are accumulated into the A memory. Accumulation into the memory will be terminated when any one of the following conditions are met:

(1) The PRESET HOLD button is depressed and the PRESET number of input cycles has been reached.

(2) The FULL SC HOLD button is depressed and any "A" memory channel reaches a full scale condition.

(3) The A ACCUM button is released.

The light above the button glows as long as the "A" memory accumulation is in progress.

3.2F B ACCUM

The B ACCUM button and light are for the B memory and function in the same manner as A ACCUM.

3.2G TEST

When the TEST button is depressed, a test signal is applied to the input. The TEST signal consists of a base level and an artificial peak in the two channels following the cursor. The artificial peak is eliminated when the cursor is set at CHANNEL = 499. The TEST signal is normally adjusted for a base level of about 100.

3.3 DISPLAY GROUP

The OMA has two basic output formats: *DIGITAL*, in which the characteristic channel number and corresponding five-digit and sign magnitude are displayed for any of the 500 OMA channels; and *GRAPHIC*, in which all 500 channels are displayed in a channel magnitude (Y) versus channel number (X) graph. The display control group, located at the right of the OMA Console, provides the functions necessary to take advantage of these capabilities. The display controls are divided into six functional subgroups as follows:

3.3A NUMERIC DISPLAY WINDOW

Light Emitting Diode (LED) numeric displays indicate the digital signal MAGNITUDE and corresponding CHANNEL number of a selected OMA channel.

The selected channel is marked by an intensified cursor dot on the 500-channel CRT display, and is available to external devices via the rear-panel CURSOR BNC connector.

DESIRED TIME	NEAREST # ACCUM CYCLES	ACTUAL TIME	ERROR
1 (Seconds)	31	1.015808	+1.58%
2	61	1.998848	-.058%
3	92	3.014656	+.489%
7	214	7.012352	+.176%
8	244	7.995392	-.058%
9	275	9.0112	+.124%
10	305	9.99424	-.058%
100	3052	100.007936	+.008%
200	6104	200.015872	+.008%
400	12207	399.998976	-.003%
500	15259	500.006912	+.0014%
700	21362	699.014848	-.0014%
800	24414	799.997952	-.00026%
900	27466	900.005888	+.00065%
1000	30518	1000.013824	+.0014%
1 (Minutes)	1831	.9999701 (Minutes)	-.003%
2	3662	1.9999402	-.003%
5	9155	4.9998506	-.003%
7	12817	6.9997909	-.003%
8	14648	7.9997610	-.003%
9	16479	8.9997312	-.003%
10	18311	10.0002474	+.0025%
20	36621	19.9999488	-.0003%
30	54932	30.0001962	+.0007%
40	73242	39.9998976	-.0003%
50	91553	50.0001450	+.0003%
60 (1 Hour)	109863 (reads 09863)	59.9998464	-.0003%

ACCUM CYCLES	TIME (milliseconds)
1	32.768 ms
2	65.536 ms
3	98.304 ms
4	131.072
5	163.840 ms
6	196.608 ms
7	229.373 ms
8	262.144 ms
9	294.912 ms
10	327.680 ms

Table III-1. INPUT TIME TABLE

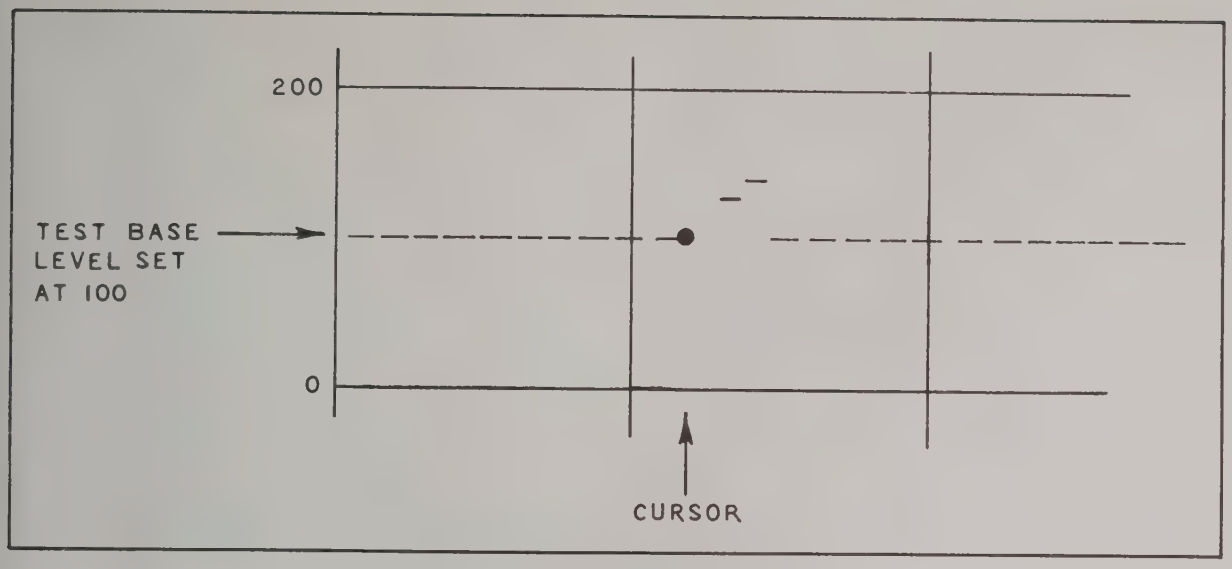


Figure III-1. CRT DISPLAY: TEST, REAL TIME

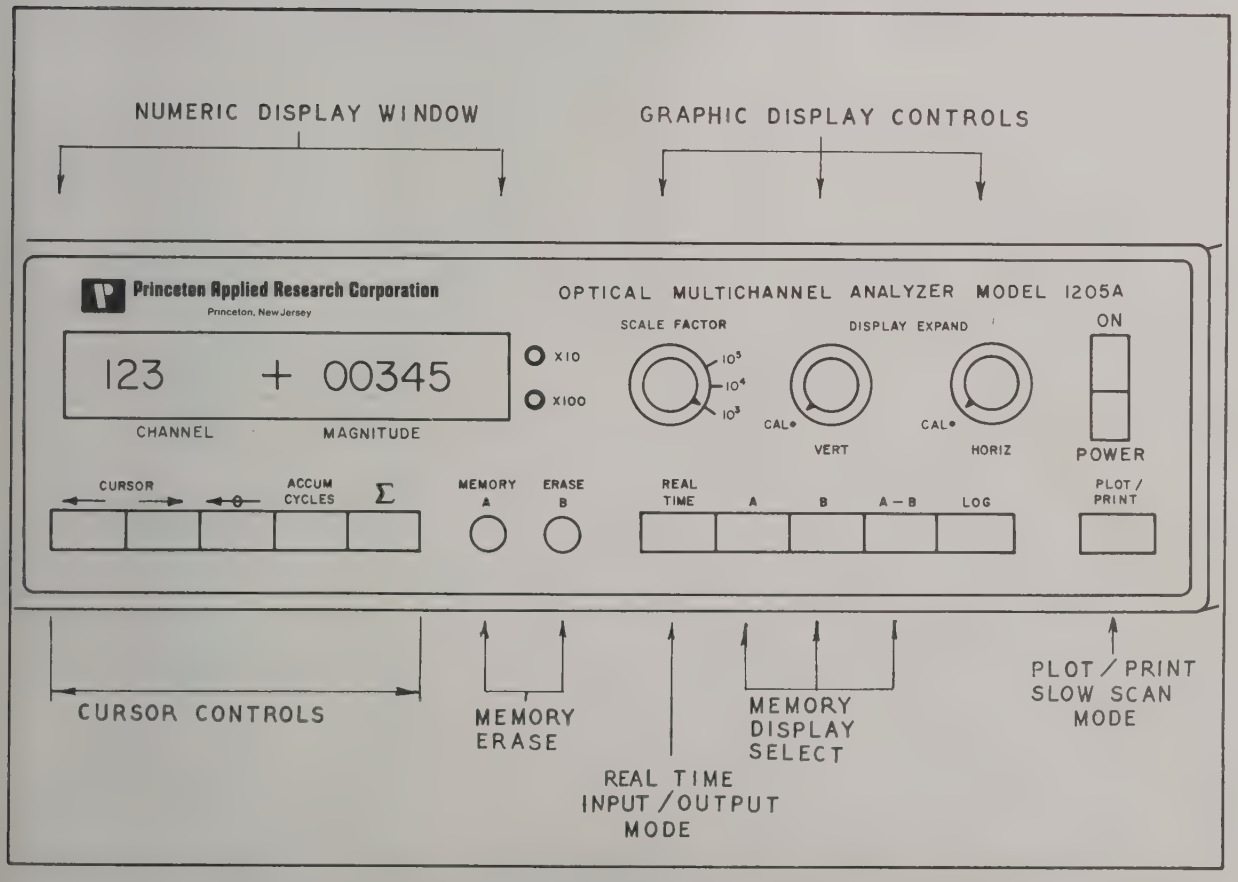


Figure III-2. O.M.A. CONTROLS

Accumulate Cycles Display
When the ACCUM CYCLES mode is selected, the CHANNEL number portion of the display is blanked out, since the number of 32.768 ms accumulate cycles is the same for all 500 channels.

X10-X100 Σ Mode Pre-Scale
One of these two lights will glow when in the summing mode (Σ) to indicate the magnitude scaling factor selected.

Error Light
The error light (located between the CHANNEL and MAGNITUDE displays) will glow if either of the following two error conditions exist:

(1) The signal input to any channel exceeds the available dynamic range (732 counts/scan).

(2) The total of the channels added together in the summing mode (Σ) causes a register overflow (i.e., exceeds the available range).

3.3B CURSOR CONTROLS

These controls comprise a group of five pushbutton switches below the numeric display window. These controls allow selection of any channel for digital display by changing the selected CHANNEL number and repositioning the intensified cursor dot on the CRT display. These controls also select two special digital readout modes: ACCUMULATE CYCLES AND Σ (channel summing mode).

Cursor Up (→) & Down (←)
Pressed momentarily, CURSOR UP (→) will advance the cursor (and the numeric display) to the next higher-numbered channel. CURSOR DOWN (←) moves the cursor to the next lower-numbered channel. After a short delay, holding either control causes the cursor to scan from channel-to-channel at a rate that will cover all 500 channels in about fifteen seconds.

An intensified dot on the CRT display indicates the position of the cursor-selected channel. This also marks the region displayed on the CRT in the horizontal expand mode (see Figure III-3).

The CURSOR UP and CURSOR DOWN controls are not available for remote programming.

Cursor Zero (→0←)
Pressing this button moves the cursor directly to channel zero.

Accumulate Cycles Mode (ACCUM. CYCLES)
Pressing this button displays the contents of a special memory counter which contains the number of 32.768 ms accumulation cycles for which the memory was active (accumulating input signal). This counter is reset when the memory is erased.

In the "A–B" DISPLAY SELECT mode the difference between the "A" memory and "B" memory accumulate-cycle counters is displayed.

The CHANNEL number in the numeric display window is blanked to indicate that this number is the same for all 500 channels. The CRT display cursor dot indicates the channel that will be displayed on return to the normal cursor mode.

Σ Channel Summing Mode
When the Σ mode button is depressed, the total number of counts in any given number of channels may be summed by moving the CURSOR over the desired channels. The summation will include the channel the cursor was on when the Σ button was depressed and the last channel the CURSOR was moved to. The total number of counts displayed must be multiplied by either X10 or X100 depending which indicator light is on. The two indicator lights are located just to the right of the display window. The X10 or X100 prescaling factor is selected by means of a rear-panel switch.

CURSOR UP (→) adds channels, and CURSOR DOWN (←) subtracts them. The sum of the channels from the initial channel to the ending channel (inclusive) will be correct provided four conditions are observed:

(1) The cursor is moved by use of the manual CURSOR UP (→) and CURSOR DOWN (←) controls *only.*

(2) Correct initial direction: If the summation is started with the CURSOR UP (→) control, the final channel must have a higher number than the initial channel. If the summation is started with the CURSOR DOWN (←) control, the final channel must have a lower number than the initial channel.

(3) Correct ending direction: The final channel must be reached from the direction of the initial channel. When summing positive (i.e., starting with CURSOR UP (→), if the desired ending channel is passed, the cursor should be moved to a channel number lower than the desired channel and then advanced to the final channel by use of the CURSOR UP control.

(4) The maximum summing range has not been exceeded. (This causes a sum mode overflow and lights the error lamp between the CHANNEL number and MAGNITUDE in the numeric display window.)

Cursor Remote Program
Two methods for programming the cursor function are provided. The cursor may be advanced to the next higher channel (or from 499 to ØØØ) by pulsing the LNADVCLKDØ input.

The cursor also can be set directly to any channel by activating the three-digit input buss PGMLN12B1. Refer to SECTION IX - INTERFACING for details.

3.3C MEMORY ERASE

Each of the two red buttons completely erases (zero's) all 500 channels of the corresponding ("A" or "B") memory.

3.3D DISPLAY SELECT CONTROLS

The DISPLAY SELECT controls are a group of five pushbutton switches that select the source of the informa-

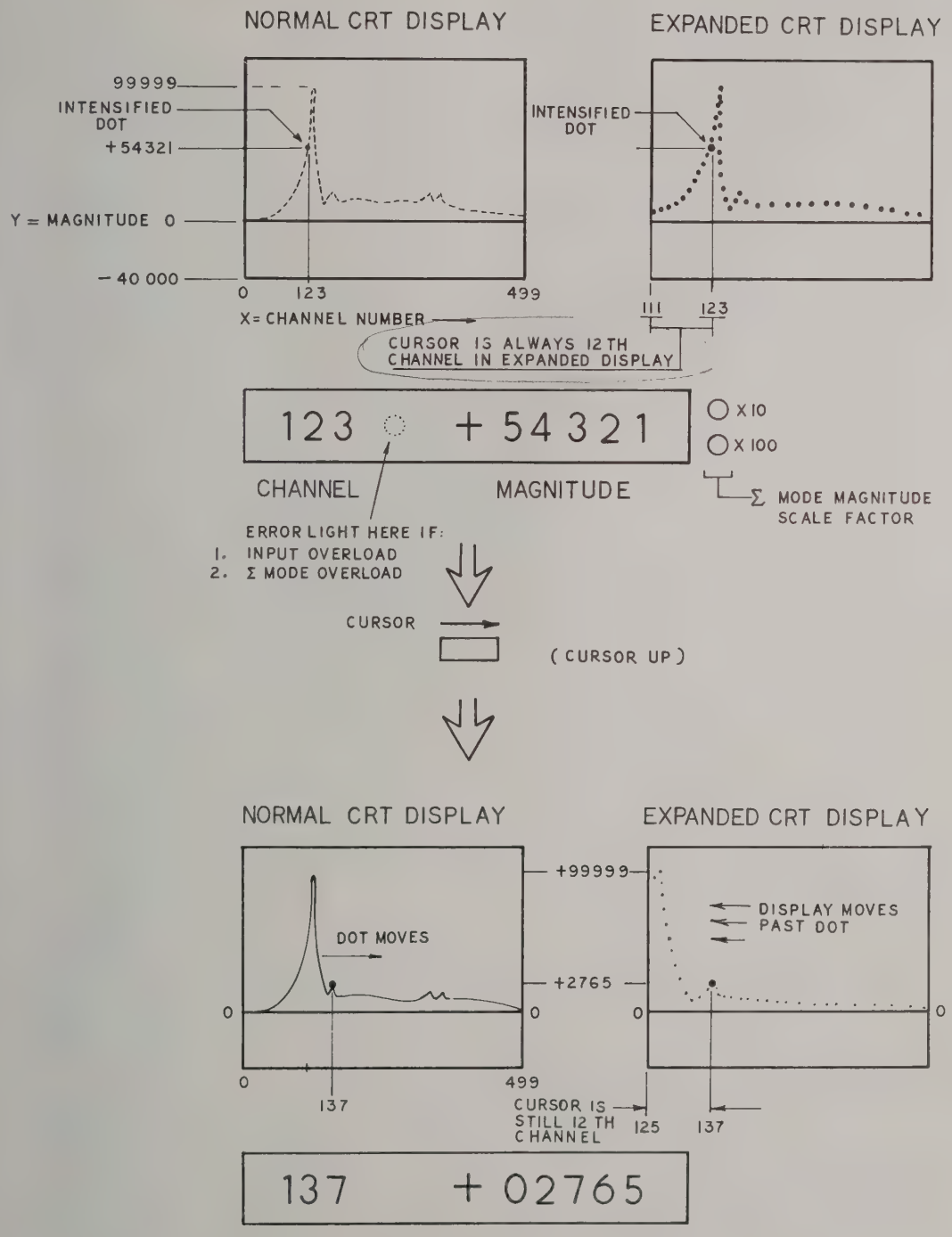


Figure III-3. CURSOR ILLUSTRATION

PLOT RATE	PER CHANNEL (ms)	500 CHANNEL PLOT SECONDS	MIN:SEC
1	32.8	16.4	
2	65.5	32.8	
3	98.3	49.2	
4	131.1	65.5	1:05
5	163.8	81.9	1:21
6	196.6	98.3	1:38
7	229.4	114.7	1:54
8	262.1	131.0	2:11
9	294.9	147.5	2:27
10	327.7	163.8	2:43
11	360.4	180.2	3:00
0	Advanced by Low-to-High TTL Transition on PRINTINHDØ (Pin 47, DIGITAL OUTPUT Connector)		

Table III-2. PLOT RATE

tion presented for digital and graphic display. Four data sources are available: REAL TIME (continuous input), either memory ("A" or "B"), or the channel-by-channel difference ("A–B") between the two memories. The fifth (LOG) switch selects log-linear magnitude scaling of any of these sources for the graphic displays only.

3.3E PLOT/PRINT MODE

Activating this mode causes the cursor to advance channel-by-channel from its initial position through channel 499. The automatic advance stops when the channel number goes from 499 to ØØØ. The advance rate is set by the rear-panel PLOT RATE thumbwheel switch (see Table III-2).

Control signals allow dumping of up to 500 channels of digital information into a printer, digital plotter, or (with the serial converter option) any ASCII-coded device.

A slow-scanning analog output (PLOT Y) and a sweep driver (PLOT X) are activated to copy the CRT display on slower graphic display devices such as plotters and chart drives.

3.3F GRAPHIC DISPLAY CONTROLS

These controls provide scale expansion in either dimension for the CRT and other graphic displays. They are located to the right of the numeric display window.

Scale Factor Control

Selects three of the five memory digits for analog output and display (identified by the associated display full-scale reading). This control is disabled in the LOG mode.

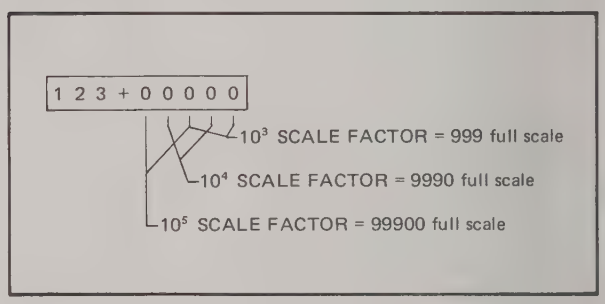


Figure III-4. SCALE FACTOR AND DISPLAY

Display Expand, Vert.

Increases the gain of the vertical output by up to X10. This control is disabled in the LOG mode. When this control is in the CAL position, the vertical output is set by internal calibration. (Normally at ±0.5 V full scale for 100 mV/div. CRT displays.)

Display Expand, Horiz.

Provides horizontal expansion of the CRT display only. When this control is in the CAL position; all 500 channels are displayed, with channel ØØØ at the left edge of the display. In any position other than CAL, the channel selected for digital display (intensified cursor dot) will be the twelfth channel from the left edge of the display. Channel ØØØ will appear to the right of channel 499, after a 12-channel blank region (see Figure III-3).

Log Mode

The LOG DISPLAY SELECT control allows the graphic

displays to show the full five decades of dynamic range on an approximate log magnitude scale. The SCALE FACTOR and VERT expand controls are disabled, producing a calibrated display.

3.4 REAL TIME MODE

Although this control is one of the DISPLAY SELECT controls in the display control group, it affects both input and output functions. When this mode is selected, it activates a continuous input mode (not stored in memory), and a real-time output mode. In the REAL TIME mode the CRT display shows the activity of 500 channels on continuous signal input, at a 32.8 ms sample rate.

3.5 EXAMPLE OF OPERATION

The following example of operation demonstrates the use of most of the OMA features in a background subtraction measurement. The signal source is assumed to be a spectrometer connected to the 1205B Detector assembly. However, the OMA's TEST mode may be used as a signal source for demonstration purposes.

Any of the display modes may be used or selected at any time to observe the measurement process, with three exceptions:

(1) REAL TIME operation inhibits accumulation into the "A" memory.

(2) Moving the cursor changes the TEST mode input.

(3) The channel summing mode (Σ) is not normally usable during memory accumulation, or while the PLOT/PRINT mode is active.

The measurement is set up using the REAL TIME mode. Signal plus background is then accumulated to full scale in the "A" memory. The ACCUM CYCLES and PRESET HOLD modes are then used to accumulate an equal interval of background only into the "B" memory. The net signal is then viewed in the "A–B" mode.

3.5A SETUP, REAL TIME

Initial conditions: All pusbhuttons except REAL TIME released, DELAY = 0, both DISPLAY EXPAND controls in the CAL position. Turn POWER on. Set SCALE FACTOR = 10^3 to observe the real time signal. About 20 seconds are required for the vidicon filament to warm up.

The REAL TIME mode is used to adjust the spectrometer for the desired spectral region and to adjust the input light level. The error LED will light up in the numeric display window if any channel has an input overload condition (over 732 magnitude). The input light level should be reduced if necessary to extinguish this indicator. The cursor is then positioned over the peak channel using the cursor controls. The digital readout allows the input light level to be set to accommodate any expected input level fluctuations. Linear overrange capability after the limit light comes on is 7% (783 magnitude) in the REAL TIME mode, or 17% (860 max. counts/scan) during memory accumulation.

If the test input mode is to be used, press the TEST pushbutton. Note that a base level of about 100 is indicated on the MAGNITUDE readouts. This will be an artificial peak in the two channels following the cursor. This peak cannot be measured directly in the REAL TIME mode as it moves with the cursor. For this example, position the cursor at CHANNEL = 250.

3.5B SIGNAL ACCUMULATION

Set the DISPLAY SELECT "A" pushbutton. (The REAL TIME mode prevents accumulation into the "A" memory.) Press MEMORY ERASE A to clear the results of any previous measurement. Both memories will have been automatically erased when the power was turned on. Set the FULL SC HOLD pushbutton.

Press A ACCUM. You are now observing the accumulation of the input signal into all 500 channels on the CRT display, and into the selected channel on the numeric display. The cursor may be moved during the accumulation to check the progress of different channels. In the TEST mode, this will also change the input peak.

Note that as the signal level exceeds 999, the CRT display overflows (folds back to zero). Set the SCALE FACTOR = 10^5 to observe the full scale memory accumulation.

When the peak channel reaches 98,000 or more, the accumulation will stop (A ACCUM indicator light goes out). The FULL SCALE indicator light (over the FULL SC HOLD switch) will light up. Release the A ACCUM switch. The FULL SCALE indicator will go out, because the memory with the full scale condition is no longer selected for input. Release the FULL SC HOLD switch. Note that if the FULL SC HOLD switch is released before the A ACCUM switch, signal accumulation will be resumed.

3.5C MEASUREMENT INTERVAL

Press ACCUM CYCLES. The MAGNITUDE portion of the numeric display will now indicate the signal accumulation time of the full-scale measurement. This time will appear as a number of 32.768 ms OMA frame cycles during which the memory was active. The CHANNEL number is blanked, as the input time is the same for all 500 channels. The INPUT TIME TABLE, Table III-1, shows the number of ACCUM CYCLES for some typical measurement times.

Set the PRESET thumbwheel switches to the ACCUM CYCLES number. Release the ACCUM CYCLES pushbutton.

3.5D PRESET BACKGROUND SUBTRACTION

Press the PRESET HOLD pushbutton. Because of the PRESET setting in the previous subsection, any memory accumulation will now stop automatically after the same input interval as was used in the just-completed full-scale accumulation.

Press MEMORY ERASE B to clear the "B" memory of the results of any previous measurement. *Turn off the signal light source.* (In the TEST mode, position the cursor at channel 499 to eliminate the artificial peak. This is conveniently done by pressing CURSOR ZERO (→0←) and then CURSOR DOWN (←).

Press B ACCUM. As the background signal is accumulated into the "B" memory, a number of observations are possible:

(1) DISPLAY SELECT "B" allows the background accumulation to be observed.

(2) DISPLAY SELECT "A–B" allows the observation of the background subtraction process. The background portions of the full scale "A" memory accumulation will appear to erode away as the accumulating "B" memory background level is subtracted out. When the background accumulation is completed (B ACCUM light out, PRESET HOLD light glowing), this display will show the effects of the signal light minus the background. (In the TEST mode, the amplitude of the peak minus the base level.)

(3) ACCUM CYCLES and DISPLAY SELECT "A–B" indicates the measurement interval status on the numeric display while retaining the CRT display as in the previous subsection. The numeric display shows the A minus B difference in the accumulation times. As the measurement goes on, this will count down to zero and stop, indicating the background accumulation time remaining before the completion of the measurement.

When the background accumulation is complete (B ACCUM light out and PRESET HOLD light glowing), release the B ACCUM pushbutton and then the PRESET HOLD pushbutton. Here again, if PRESET HOLD is released before B ACCUM, background accumulation will be resumed.

3.5E MEASUREMENT OUTPUT

In the "A–B" DISPLAY SELECT mode, the magnitude-versus-channel number plot on the CRT display represents a signal-versus-wavelength plot of the spectrometer output. Spectral lines may now be identified by positioning the cursor over the peaks on the CRT display and reading out the channel number and magnitude. If a spectral line is spread over several channels, the signal may be totaled by use of the Σ mode as described previously. If a printer is connected, its PRINT ONCE control may be activated at any time to record the numbers being presented in the OMA's numeric display window.

The following is one method for recording the data when both a printer and a plotter are connected. Position the cursor at CHANNEL = 000 (◄0 control). Activate the plotter, and set the printer in the STANDBY mode. Press the OMA's PLOT/PRINT pushbutton and follow the progress of the plotter by observing the position of the cursor dot on the CRT display. As the cursor approaches a spectral peak, switch the printer from STANDBY to OPERATE until the peak is passed. When the cursor returns to CHANNEL = 000 and stops, raise the plotter pen and then release the PLOT/PRINT control. This records the significant data without wasting a lot of printer paper on empty channels.

SECTION IV
OPERATION

4.1 PRELIMINARY CONSIDERATIONS

For convenience, the following assumptions will be made in describing the operation of the Model 1205 Optical Multichannel Analyzer.

(1) The instrument is being used with the recommended Tektronix #604 X-Y CRT Display, or equivalent. A wide variety of other X-Y or general purpose scopes could also be used, in some cases with a loss in operating convenience. This capability is covered in detail in Section VII – USE OF NON-STANDARD DISPLAY SCOPES.

(2) The Detector Head Assembly is a standard 1205B, properly aligned and focused, with an input signal from a spectrograph or polychromator. This signal is a portion of a spectrum with wavelength dispersed along the frame scan (CHANNEL NUMBER) direction, and each spectral line appearing as a 0.2 in. long slit image on one or more of the 0.2 x 0.001 in. channel elements. Optical alignment and focusing of this and other patterns is covered in Subsection 4.5. The detector head drive electronics are correctly adjusted at the factory for this application unless the OMA is ordered with, and/or calibrated for, some other device. The electronic alignment is covered in Section VIII - ADJUSTMENT OF DETECTOR HEAD ELECTRONICS.

Almost all of the OMA operating parameters may be demonstrated in the absence of the above input by using the TEST input mode. Exceptions are the input limit light (Subsection 4.6A), vidicon signal integration delay (Subsection 4.6B) and, of course, the optical input alignment (Subsection 4.5).

(3) The printer used is the P.A.R.C. Model 5055A-H49 with printer cable #110380. Information for interfacing the OMA with other printers is provided in Section IX – INTERFACING.

(4) Unless otherwise noted, the OMA controls are set as follows:

Pushbuttons: all released except A DISPLAY SELECT
Delay: Ø
Preset: ØØ1Ø
Scale Factor: 10^5
Vert. Expand: CAL
Hor. Expand: CAL
Plot Rate (rear panel): 9

4.2 MEMORY INPUT OPERATION

4.2A A AND B ACCUMULATION

The A ACCUM and B ACCUM Input Control switches are the primary controls for most OMA measurements. Pressing one of these input controls initiates the accumulation of input signal information from the Detector Head (or TEST input) into the corresponding 500 channel memory. This signal accumulation continues until the A ACCUM or B ACCUM switch is released, or until the measurement is automatically terminated by the PRESET HOLD or FULL SCALE HOLD modes. The same signal is accumulated into both memories when both A ACCUM and B ACCUM are active at once.

During each detector scan the light signal integrated on each of the 500 vidicon target elements since the last scan is converted into a digital value and added to the contents of the corresponding five digit and sign MAGNITUDE word of the selected 500 word memory. If the memory is selected for display by the corresponding "A" or "B" DISPLAY SELECT control, the growth of the accumulating signal levels can be observed on the CRT and numeric displays as the measurement progresses. Although these controls are operated asynchronously, the actual measurement is synchronized with the instrument's internal 32.8 ms (actually 32.768 ms or 2^{15} μs) accumulation cycle. This is done to assure equal signal input time into each of the 500 channels.

When an integration DELAY is used, the measurement will always consist of a number of complete input cycles, each consisting of a number of 32.768 ms accumulation cycle intervals. The total number of such intervals accumulated into each memory may be observed on the OMA numeric display by pressing the ACCUM CYCLES cursor control. Since this value is the same for all 500 channels, the CHANNEL number is blanked in this display mode. These controls may be operated in synchronism with external events by use of the OMA's remote program capabilities.

4.2B FULL SCALE HOLD

Each of the two OMA memories has a full-scale sensor which is activated when any of the 500 channels in that memory reach +98000 or more. If a memory in this condition is selected (A ACCUM or B ACCUM), the FULL SCALE input control status lamp will glow.

If the FULL SC HOLD Input Control pushbutton is in the depressed position when a FULL SCALE condition is sensed, the input into both memories will be terminated on completion of the 500 channel scan in progress. Because full scale detection takes place at 98000, completion of the in-progress scan will not cause a memory overflow in any channel, and equal signal input times for all 500 channels are maintained.

4.2C PRESET HOLD MODE

The preset hold mode is controlled by the PRESET HOLD Input Control switch, the four PRESET digits of the thumbwheel switch, and an internal counter which counts the number of input cycles scanned into the memory. When the counter reaches the PRESET value, further input into either memory is inhibited.

The preset counter has three basic states in its operation:

(1) Reset: The counter is held at zero while the PRESET HOLD button is released. It is also reset when either MEMORY ERASE button is pressed.

(2) Active: PRESET HOLD is set, but the counter is not yet at the PRESET value (PRESET HOLD status lamp not illuminated). In this condition the preset counter will count each input cycle into either memory. Note that each input cycle counted may consist of one or more 32.768 ms ACCUMULATION CYCLES, depending on the vidicon integration delay used.

(3) Preset Hold (PRESET HOLD status lamp illuminated): The counter is at the PRESET value, preventing further input into either memory, and thus holding the preset counter at the preset value.

The preset hold circuit may be used in a number of ways, depending on the application. A discussion of each follows.

(1) Normal PRESET Measurement

Before the measurement is started (by pressing A ACCUM and/or B ACCUM), the PRESET thumbwheel switches should be set for the desired measurement interval. The preset counter is initialized by erasing a memory or by releasing the PRESET HOLD push-button and then setting it again.

The measurement is initiated by setting A ACCUM and/or B ACCUM and will be automatically terminated after the preset interval. The measurement may be interrupted any number of times by releasing the A ACCUM and B ACCUM controls, without affecting the total signal input time accumulated into the memory by the PRESET HOLD.

(2) Changing the PRESET Value

The setting of the PRESET switch may be changed during a measurement, and the PRESET HOLD will occur at the new PRESET time. If a PRESET HOLD has already occurred, the accumulation process will restart and continue until the new PRESET value is reached. It is normally possible to increase the measurement interval one input cycle at a time by advancing the setting of the PRESET switch.

Note that the new PRESET setting must be completed before the input process arrives at that level. For example, after the PRESET HOLD has reached a PRESET of 99, if the switch is changed to a PRESET of 9Ø instead of a PRESET of 1ØØ, the measurement will restart and continue until 1ØØ9Ø input cycles have been completed. Releasing the A ACCUM and B ACCUM switches will avoid the possibility of the measurement getting ahead of the PRESET switch change. When the new PRESET setting is completed, the measurement is restarted by setting A ACCUM and/or B ACCUM.

(3) Adding a PRESET Interval

The PRESET HOLD mode may be used to add a succession of PRESET intervals, to sum a group of short term measurements, or to increment an existing measurement. With A ACCUM and B ACCUM released to prevent unwanted input, release PRESET HOLD and then press it again. This resets the PRESET counter. When the measurement is restarted by setting A ACCUM and/or B ACCUM, the PRESET number of input cycles will be added to the existing measurement stored in memory.

(4) Simultaneous Start Control of A and B ACCUM

The PRESET HOLD mode may be used to provide simultaneous control of input into both memories. This avoids the problem of synchronizing the actuation of the A ACCUM and B ACCUM controls. The method is as follows:

(a) With both A ACCUM and B ACCUM released, set the PRESET to ØØØØ, and set the PRESET HOLD control. The PRESET HOLD status lamp should be lit. Set both A ACCUM and B ACCUM. In this condition, signal from the detector head will be accumulated into both memories simultaneously, starting with the release of the PRESET HOLD mode control, or a change in the PRESET setting.

(b) Setting PRESET HOLD again will stop input to both memories, but this is not recommended as accumulation will stop in mid-cycle resulting in more signal in early channels than in the rest. Changing the PRESET setting will result in a simultaneous start and a PRESET HOLD stop.

(5) PRESET Control by MEMORY ERASE

Pressing either MEMORY ERASE button will simultaneously clear the corresponding memory and zero the PRESET counter. Thus if the ACM control is left set at the end of a normal PRESET measurement into a memory, pressing and releasing the MEMORY ERASE control for that memory will initiate a complete new PRESET measurement.

While both the ACCUM and MEMORY ERASE controls for the same memory are set, the OMA operates in a mode similar to the REAL TIME mode. This mode may be used to observe the input signal while the MEMORY ERASE control is held in until the signal of interest is observed to begin. Releasing the MEMORY ERASE control will then initiate the PRESET measurement.

If the input cycle includes an integration delay, the ACCUM CYCLES readout may be incorrect. The ACCUM CYCLES number may be too small by up to the number of accumulation cycles in one integration delay. However, the actual measurement interval will

be the correct time as determined by the PRESET HOLD mode.

(6) PRESET Input Cycle Defined

The PRESET HOLD mode counts OMA input cycles. The nature of this input cycle depends on the mode of OMA operation.

In normal (DELAY = Ø) operation, the vidicon is scanned continuously, and each 32.768 ms frame time accumulated into memory is a complete input cycle. In this mode, the change in the ACCUM CYCLES reading will equal the PRESET number.

If an integration delay is used (DELAY ≠ Ø), the input cycle consists of a number of non-scan signal integration frame times set by the DELAY switch, followed by a readout scan. In this mode the measurement time (in 32.768 ms ACCUM CYCLES) is (PRESET) X (DELAY + 1).

If the 1207 Extended Delay Accessory is used, each input cycle is a number of seconds set by the 1207 DELAY SECONDS control. The OMA crystal is changed with this option to provide exactly 31 frame times per second, and the frame time in all normal modes becomes 1/31 second. The PRESET measurement time becomes (PRESET) X (1207 DELAY SECONDS) seconds. The ACCUM CYCLES reading will be (PRESET) X (1207 DELAY SECONDS) X (31).

When the 1205A console is modified for the 1207, the signal integration time in non-extended delay measurements is (ACCUM CYCLES MAGNITUDE)/31 seconds.

(7) Exchanging Preset and Delay Switches

Internal switches in the 1205A OMA console (on the PRESET card) interchange the PRESET and DELAY functions to allow the long vidicon integration delays possible with cooled vidicons. In this mode, the PRESET switch mentioned in the previous paragraphs is the single thumbwheel digit, and the four-digit group becomes the DELAY switch.

4.2D DURING REAL TIME OPERATION

The REAL TIME mode uses the "A" memory counter, and the "A" memory cannot be augmented while the OMA is in the REAL TIME mode. However, all normal memory operations are possible using the "B" memory, while observing the input signal in the REAL TIME mode.

4.3 OUTPUT MODES

4.3A CRT DISPLAY

The Cathode Ray Tube (CRT) display provides simultaneous display of all 500 channels in (intensity vs channel number) graphic form. The speed of this device allows observation of the real-time activity in all 500 channels. The 500 channel presentation allows convenient selection of areas of interest for digital output.

In the following discussion the use of an X-Y display with Z (intensity) axis modulation, such as the Tektronix 604 provides, is assumed. It is also assumed that the display and 1205A have been calibrated as per Section VI. Refer to Section VII for information on the use of non-standard display scopes.

(1) Setup

(a) Check that the CRT display is adjusted for the local ac power source voltage (refer to the display instruction manual for proper setting).

(b) Apply power to the CRT display.

(c) Set the CRT display intensity control for a visible dot. Position this dot at the left edge of the display, two divisions up from the bottom of the 8 x 10 division display area (see Figure IV-1).

(d) Reduce the intensity setting until the dot is just extinguished.

(e) Connect the CRT X, CRT Y, and CRT Z outputs on the back panel of the OMA to the corresponding X, Y, and Z inputs on the CRT.

(f) Set "A" DISPLAY SELECT on the OMA console. Release all other switches, and set both DISPLAY EXPAND controls to the CAL position.

(g) Turn the OMA POWER on.

(h) Adjust the CRT display Intensity control for a comfortable viewing level.

(i) Adjust the CRT display vertical position control to move the baseline over the graticle line two divisions up from the bottom of the display.

(2) Normal Display

The Normal CRT Display format is shown in Figure IV-1. Channel ØØØ is at the left of the display. The vertical scale factor is calibrated so that five divisions will represent 10^3, 10^4, or 10^5 counts magnitude, depending on the setting of the SCALE FACTOR control. The DISPLAY SELECT pushbuttons on the 1205A front panel select the real-time input, memory A, memory B, or the channel-by-channel difference (A–B). The SCALE FACTOR should be set at 10^3 when the real time display mode is selected. An intensified cursor dot marks the channel selected for digital display.

(3) Scale Factor

The SCALE FACTOR control selects three of the five available MAGNITUDE digits for display on the CRT.

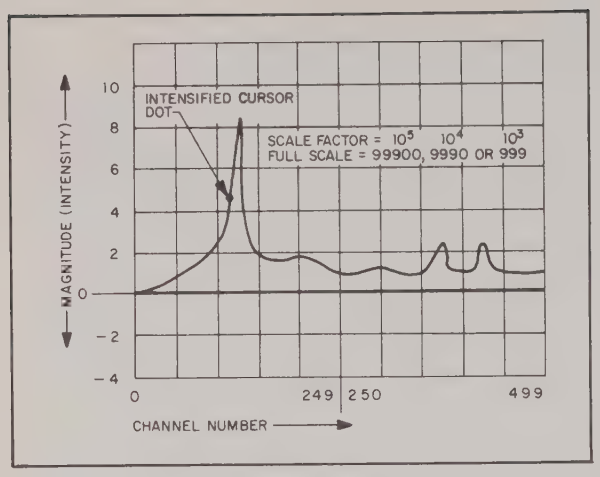


Figure IV-1. NORMAL CRT DISPLAY

This allows the available CRT display resolution to be optimized for high or low level signals. When a channel's magnitude exceeds the SCALE FACTOR setting, the display is folded. If a SCALE FACTOR of 10^3 were used, a magnitude of 01200 would appear one division above the zero line (= 200). A SCALE FACTOR of 10^5 is normally used for the full-scale hold mode, while a SCALE FACTOR of 10^3 is required to view the less than 800 counts of the real time mode.

(4) Vertical Scale Expand

This control increases the CRT display vertical gain by a factor of from X1 to X10 when not in the CAL position.

(5) Cursor

The channel selected for digital display (in the numeric display window) is marked by an intensified dot on the CRT display. This dot also marks the region that will be on the screen in the horizontal display expand mode. The cursor up (→), cursor down (←), and cursor zero (◄0►) controls are used to position the cursor over points of interest on the display. When the cursor up (→) control is pressed in the non-expanded mode, the intensified dot moves to the right, toward higher channel numbers.

(6) Horizontal Scale Expand

The Horizontal Scale Expand control can expand the CRT display by up to 10 times. The expanded region shown on the CRT display is selected by the cursor as follows: If the HORIZ SCALE EXPAND control is *not* in the CAL position, the cursor selected channel will be the twelfth channel from the left edge of the screen. When the cursor is moved using the cursor controls, the 500 channel display will appear to flow past a fixed cursor dot. There is a 12 channel wide blanked region between channel 499 and channel ØØØ which may appear on the screen in this mode. If the cursor is at channel ØØØ while in the Horizontal Expand mode, this will appear as though the display were displaced slightly to the right.

(7) LOG Mode

Pressing the LOG display select pushbutton provides a logarithmic intensity scale on the CRT display. The LOG control disables the SCALE FACTOR and VERTICAL SCALE EXPAND controls, so that the log mode CRT display will always be calibrated as

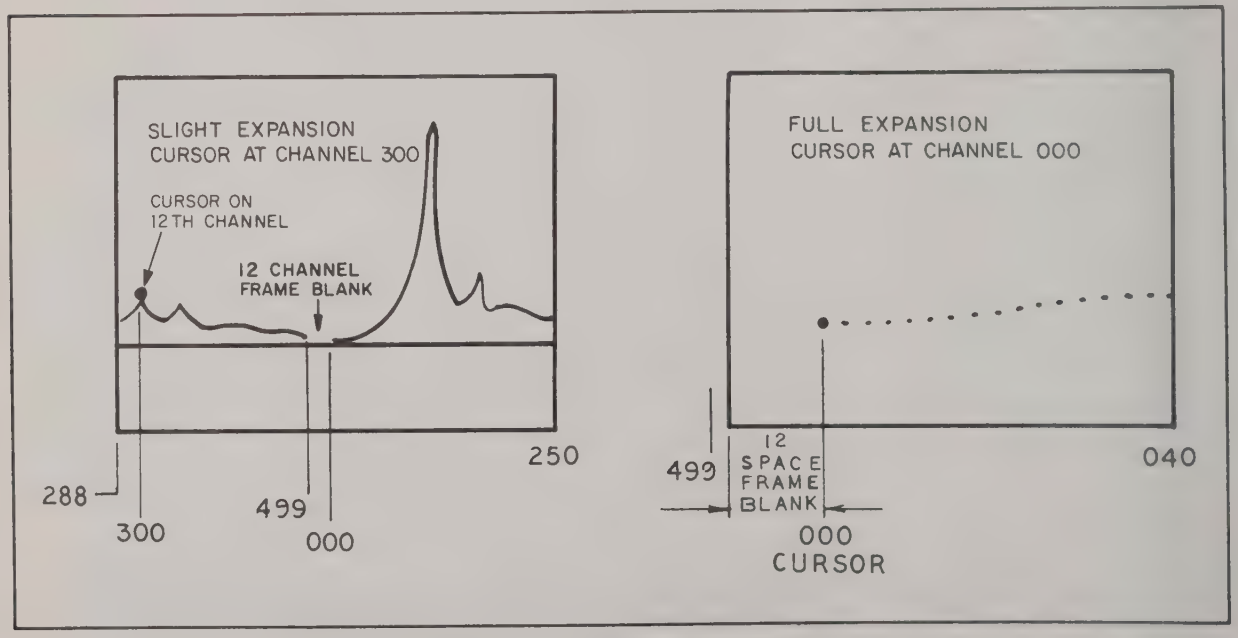


Figure IV-2. HORIZONTAL EXPANSION

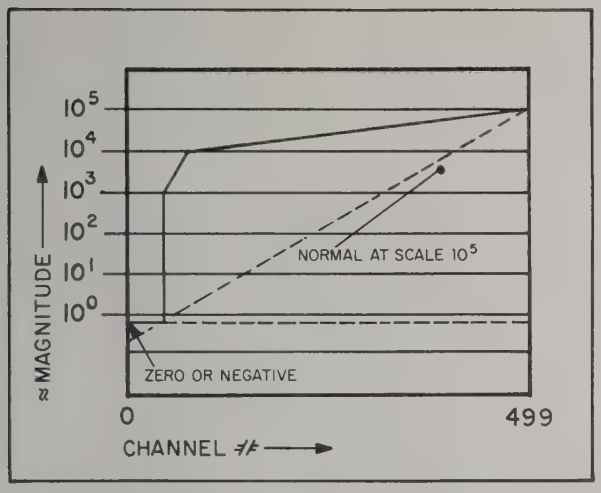


Figure IV-3. LOGARITHMIC DISPLAY

indicated in the figure above. The digital outputs are unaffected by the log mode. The log mode is actually an approximation in that there is linear interpolation between logarithmic decades (linear approximation of mantissa). This results in data which may be easily read, but which differs by ±3% from the true log. The log mode allows the CRT display to show the full five decades of the memories' dynamic range.

4.3B CHART DRIVE/PLOTTER

The plotter mode is activated by pressing the PLOT/PRINT button on the OMA front-panel. This activates a sweep ramp output (PLOT X) and an output (PLOT Y) that follows the magnitude of the cursor-selected channel as the cursor is automatically advanced from channel-to-channel. These outputs allow a plotter or chart recorder to provide a hard copy of the CRT display. Use of this mode also allows a plot of the real time activity or memory accumulation of a single channel when the plot rate is adjusted to "0".

(1) Setup: MAGNITUDE Axis

When active, the PLOT Y output produces twice the voltage of the CRT Y output. The CRT display setup should therefore be completed before setting up the plotter or chart drive. The standard factory adjustments (CRT Y = 100 mV/div, PLOT X = 10 mV/s) are intended to produce a 10-by-15 division plot of positive region of the CRT display in 2-1/2 minutes on a 100 mV/division plotter, with an OMA PLOT RATE setting of 9. The setup procedure follows:

(a) OMA Console: Set display select "A", SCALE FACTOR to 10^5, VERT DISPLAY EXPAND to CAL, and erase the "A" memory. Press PLOT/PRINT.

(b) Connect the OMA output PLOT Y to the Y (magnitude) axis input of the plotter (chart drive).

(c) Adjust the plotter's Y position control to locate the pen over the desired zero line.

(d) For initial setting: press TEST, FULL SCALE HOLD, and then A ACCUM. Observe the plotter as the OMA integrates to full scale and adjust the plotter's Y axis gain as necessary to prevent limiting.

(e) Release A ACCUM and PLOT/PRINT, and erase the "A" memory. Move the cursor to CHANNEL 499 to eliminate the TEST peak. Set TEST, FULL SCALE HOLD, and then A ACCUM.

(f) When the accumulation is complete (FULL SC HOLD indicator glowing, A ACCUM indicator out), press PLOT/PRINT and adjust the plotter's Y axis gain control to position the pen over the desired full scale line corresponding to the MAGNITUDE reading.

(2) Setup: Chart Drive

Select a PLOT RATE setting (OMA rear panel) using Table III-2 (PLOT RATE). Three basic requirements must be met:

(a) The PLOT RATE setting must allow enough time per channel to accommodate the slew rate and settling time requirements of the recorder. Note that the magnitude can go from zero to full scale on successive channels.

(b) The PLOT RATE setting and the chart drive rate must be compatible.

(c) If simultaneous printer and chart recorder operation is desired, the time per channel must exceed the asynchronous cycle time of the printer.

The PLOT/PRINT control signal P/PSWDØ is available on the rear-panel DIGITAL OUTPUT connector, and may be used to activate the chart drive and/or pen lift. See Section IX – INTERFACING, for details.

(3) Setup: Plotter X Axis

PLOT X is an output designed to drive the X (channel number) axis of an X-Y plotter. This output starts at zero volts when the PLOT/PRINT mode is activated and goes positive at a nominal rate of 10 mV/s until the 500 channel plot is completed or a limit is reached at just over +2 V. The setup procedure is as follows:

(a) Set display select pushbutton "A". Release all other pushbuttons. Set CHANNEL = ØØØ (press ~~→0←~~).

(b) Connect the OMA output PLOT X to the X axis input of the plotter.

(c) Adjust the plotter's X position control to locate the pen over the desired channel origin.

(d) Select a suitable PLOT RATE.

(e) Press the PLOT/PRINT control. As the plotter pen and the channel number advance, adjust the plotter's X axis gain control so that the pen is always slightly ahead of the desired position as indicated by the channel number. (Setting gain slightly above the desired level.)

(f) When the pen is over the desired location for channel 499, start reducing the gain as necessary to hold the pen at that point. Stop adjusting the gain when the channel number advances from 499 to ØØØ and stops. At this point the PLOT X sweep will stop.

(g) Release the PLOT/PRINT control. This will cause the pen to return to the channel ØØØ position. Check the plotter X-axis gain adjustment by pressing PLOT/PRINT again and observing the correct relationship between pen position and channel number.

(h) If necessary, the PLOT X ramp rate may be altered to suit the plotter requirements. See Section VI.

(4) Setup: Incremental & Digital Plotters

The digital outputs and control signals normally used to operate printers are also suited to the operation of digital or incremental plotters. In particular, the print command (PRINTCMDDØ) provides a pulse for each channel in the PLOT/PRINT mode which may be used to advance incremental chart recorders. See Section IX - INTERFACING for information on this application.

(5) Plotter Operation

Once the initial setup has been completed, plotter operation proceeds as follows:

(a) Use the SCALE FACTOR, DISPLAY SELECT, and VERT DISPLAY EXPAND controls to display the desired output on the CRT. Note that the VERT DISPLAY EXPAND control also expands the plotter output, and (if the Log mode is not to be used) could have been used instead of the plotter's Y axis gain control in steps d and f of the MAGNITUDE Axis Setup Procedure (4.3B-1). However, use of the VERT. EXPAND control in this way would require calibration every time the control were changed in order to view the CRT display. If the VERT DISPLAY EXPAND control is used to expand the plotter output, care should be taken to see that any channels expanded off the CRT display do not cause plotter input overload or limiting.

(b) Position the cursor at the left edge of the region to be plotted. This is normally channel ØØØ — press the CURSOR ZERO (⊸0⊸) control momentarily.

(c) Activate the plotter or chart recorder.

(d) Press PLOT/PRINT. The plotter or chart recorder will duplicate the CRT display. The cursor dot on the CRT display will follow the progress of the plotting operation.

(e) When the channel advance goes from channel 499 to channel ØØØ, it will stop, holding the magnitude of channel ØØØ. If the plotter is operating on the PLOT X sweep output, the sweep will stop. Raise the pen and release the PLOT/PRINT control to return the plotter to the zero-zero position.

(f) The plotting operation may be stopped at any time by releasing the PLOT/PRINT control.

(6) Channel-vs-Time Plot

If the PLOT RATE is set at zero, or the cursor is locked on a single channel by use of the remote program inputs, the plotter or chart recorder will record that channel as a function of time in the REAL TIME or memory accumulation modes. The PLOT/PRINT button must be set in order to activate the PLOT Y output.

(7) Simultaneous Print and Plot

Simultaneous printer and plotter operation is possible if the PLOT RATE setting allows enough time per channel for the completion of the printer cycle (see Table III-2, PLOT RATE).

(8) Serial Converter Conflict

The Serial Converter, when installed and activated, disables the PLOT RATE control and provides its own channel advance signal. Even if the channel rate set by the serial converter were compatible with the plotter, the serial converter pauses after every fifth channel to output a channel number. This would result in a nonlinear X (MAGNITUDE) axis scale factor. Thus, use of the plotter and the serial converter will normally require two passes over the memory data.

4.3C PRINTER

The following section refers to the operation of the P.A.R.C. accessory printer Model 5055A-H49. **CAUTION:** See Subsection 4.3C-3. If other printers are to be used refer to Section IX for interface information. The operating instructions will apply for most printers.

(1) Installation

(a) Plug in the cable (#110380) to the 1205A TTL DIGITAL OUTPUT connector and the printer connector. Note that the connectors used are identical and the two ends of the cable are interchangeable. It is worthwhile on first installation to clean the contacts on the cable and

CHANNEL NUMBER	SOURCE CHAR.	SIGN CHAR.	MAGNITUDE	SOURCE	SIGN	MODE
1 2 3	A	+	1 2 3 4 5	A memory	+	A
1 2 3	B	–	1 2 3 4 5	B memory	–	B
1 2 3	D	+	2 4 6 9 0	Difference	+	A-B
1 2 3	A	P	1 2 3 4 5	A mem. sum	+	Σ, A
1 2 3	B	N	1 2 3 4 5	B mem. sum	–	Σ, B
1 2 3	A	T	1 2 3 4 5	A Time	+	ACCUM CY, A
1 2 3	B	T	1 2 3 4 5	B Time	+	ACCUM CY, B
1 2 3	D	T	1 2 3 4 5	(A-B) Time	+	ACCUM CY, A-B
1 2 3	D	*	1 2 3 4 5	(A-B) Time	–	ACUM CY, A-B
1 2 3	*	+	0 0 3 4 5	* = REAL TIME	+	REAL TIME

Table IV-1. DIGITAL RECORDER FORMAT TABLE

equipment connectors with a cotton swab dipped in alcohol to remove any possible accumulation of dust, smog, etc., which may have settled on the 200 contacts involved.

(b) Set the switches on the back of the printer as follows:

(i) LINE SELECTOR to 115 or 230 as appropriate for the ac line voltage used.

(ii) ±8421 switch to +8421.

(iii) BLANKING to OFF.

(c) Plug in the printer and 1205A to the ac line and turn on the power in both units.

(2) Format

The printer output format consists of a three-digit channel address, a character indicating the memory source of the data, a sign character, and a five-digit number representing the magnitude of the selected channel. The following examples illustrate the printer output format:

Note that the source character indicates the choice of the "A", "B", "A–B", or REAL TIME (A, B, D, and *) memory DISPLAY SELECT modes.

The sign character indicates the sign associated with the MAGNITUDE, and is modified to indicate the special (non-channel magnitude) nature of this number in the integrate (Σ) and ACCUM CYCLES modes.

The integrate (Σ) mode is indicated by replacing the normal (+ or –) sign notation with (P or N) to indicate a positive or negative summation. In this case the CHANNEL NUMBER is the number of the ending channel in the summing process, and the MAGNITUDE is the sum of some number of channels. The Σ mode magnitude scaling factor (X10 or X100) indicated on the front panel display is not printed out.

The ACCUM CYCLES mode is indicated by replacing the normal (+ or –) sign notation with (T or *) to indicate positive or negative time. In this case the MAGNITUDE represents a number of frame times. Note that the ACCUM CYCLES time indication is always a positive number or zero (sign character = T) for the "A" memory or "B" memory DISPLAY SELECT modes. This number can go negative (sign character = *) in the difference (A–B) mode, but the normal application of the ACCUM CYCLES difference mode calls for the difference to be zero (sign character = T).

In the ACCUM CYCLES mode the channel number is blanked on the display, since the ACCUM CYCLES value is the same for all channels within a memory. However, the printer will print a channel number in this mode. The channel number printed in the ACCUM CYCLES mode has no significance whatever.

Except as noted above, the CHANNEL NUMBER and MAGNITUDE portions of the printout will correspond exactly to the front-panel display on the 1205A.

(3) Standby Mode

Setting the printer's OPERATE/STANDBY switch in the STANDBY position will inhibit printing. This mode is useful when the PLOT/PRINT mode is used to operate an analog plotter, if digital printout is not required, or is required only for selected channels. *The printer POWER switch should not be used for this purpose, as operating the OMA with the printer connected but turned off may cause the OMA to produce faulty output codes.* This may also produce

incorrect or blank characters in the front-panel numeric display.

(4) Automatic PLOT/PRINT Mode

When the PLOT/PRINT switch is depressed, the printer will commence printing the contents of the selected memory at a rate determined by the back panel PLOT RATE switch (if the printer is not in the standby mode). This switch may be set for any rate which does not exceed the 10 lines/second maximum rate of the printer. In practice, this allows any PLOT RATE setting of "4" or larger (4 = 4 OMA frame times/channel = 130 ms). The rate may be selected to allow simultaneous printing and plotting of the selected output (see Table III-2, PLOT RATE).

The first channel printed will be the channel indicated prior to the activation of the PLOT/PRINT switch, and all higher-numbered channels will be printed in sequence until the PLOT/PRINT switch is released or channel 499 is printed out.

The PLOT/PRINT operation may be started at channel number ØØØ by activating the cursor zeroing switch momentarily (⊣0⊢) or LNZERODØ @ DIG. OUT Pin #49) prior to activating the PLOT/PRINT cycle.

(5) Interactive PRINT Mode

If the PLOT RATE switch is set at zero, the PLOT/PRINT cycle will operate in the interactive mode. In this mode the end of the "printer busy" signal (PRINTINHDØ, TTL DIGITAL OUTPUT connector Pin 47) advances the channel number and, in the PLOT/PRINT mode, generates a new print command.

When the PLOT/PRINT switch is activated in this mode, the information from the starting channel through channel 499 will be printed out as in the automatic print mode, but at the maximum rate of which the printer is capable.

This mode is not suitable for simultaneous printing and plotting of the data, since the time per channel is partially dependent on the instantaneous phase relationship between the OMA and printer operating cycles. This is also the cause of the characteristic slightly ragged sound of the printer in this mode.

(6) Manual Print Mode

If at any time the printer is not in STANDBY, and its MANUAL PRINT button is depressed, the printer will print out the data then being displayed by the OMA. This is the method best suited to printing ACCUM CYCLES or Σ mode data. It is also useful in conjunction with the cursor controls to print out selected peak information without wasting paper on unwanted baseline channels.

If the OMA is set up for interactive printing (PLOT RATE = Ø), the channel number will be advanced after the manual print operation is completed. This is an acceptable method for printing out a selected group of channels in sequence. In the Σ mode, however, the channel number advance associated with an interactive manual print does not allow enough time for the full channel summing cycle. Thus, although the manual print correctly produces the result of a Σ summing operation performed using the cursor controls, it then advances the Σ operation to a new and incorrect state (see cautionary notes below).

(7) REAL TIME Mode

Unless the input signal level is extremely stable, the REAL TIME mode output data will be fluctuating at a rate too high for the printer to follow. In addition, each channel printed out would be from a different set of scans than the previous one. For this reason the recommended approach is to print from a memory the results of PRESET HOLD = 1 accumulation. This will hold the results of a single real time scan.

An exception is the case where the measurement application calls for a vidicon integration delay of three or more frame times. In this case the selected channel output will be stable long enough for a correct printout. However, it will still be true that successive printouts will be from different vidicon scans.

(8) Cautionary Notes

(a) Power Off Operation. When the printer power is turned off, the printer inputs present an improper load condition on the OMA outputs. This will not cause any damage, but may cause the OMA to function improperly, particularly in the Σ mode. The malfunction usually appears in the form of plausible but incorrect output numbers. If the printer is not to be used, it should be left in the STANDBY mode, or it should be disconnected from the OMA.

(b) Interactive Manual Printing in the Σ Mode. When the OMA PLOT RATE switch is set at zero and the printer's MANUAL PRINT button is pressed (interactive manual print mode), the printer will print the current data and then advance the channel number. In the Σ mode this will *appear* to produce a succession of partial sums as the channel number is advanced.

Unfortunately, advancing the channel number in this manner does not allow time for the complete summing process. Even moderate channel magnitudes will be truncated. This is a consistent error, and the Σ mode will appear to be operating correctly, but the numbers printed will be incorrect.

(c) Running Out of Paper. Approximately 15 sheets of fanfold paper are required to print 500

channels. If the paper runs out in the middle of a PLOT/PRINT operation, printing and the channel number advance will stop automatically.

Place the printer in STANDBY or release the PLOT/PRINT switch before loading more paper. If this is not done, the OMA may be advanced through several channels during the loading operation. Should this occur, the cursor controls may be used to return the OMA to the channel at which printing was discontinued before restarting the PLOT/PRINT operation.

4.4 REAL TIME MODE

Although the REAL TIME mode is selected by one of the DISPLAY SELECT pushbuttons, it is in fact a combined input and output mode. When this mode is selected, the input circuits and integration delay control are activated as for a memory accumulation, but the signal is passed through to the output circuits without being added to memory. Special characteristics of the REAL TIME mode are as follows.

4.4A SCALE FACTOR

The REAL TIME mode requires a SCALE FACTOR setting of 10^3 for the best CRT display. The error light will light to indicate input overload if any channel reaches the 732 level, and an improper display will result when the 7% real time linear overrange (783) is exceeded.

4.4B NUMERIC DISPLAY

To improve the readability of the least significant digit, the numeric display is updated three times a second (every tenth cycle) in the REAL TIME mode. However, the digital outputs at the rear panel continue to be updated after each input scan.

4.4C INTEGRATION DELAY

When an integration delay is used (DELAY $\neq$ Ø), the CRT display will follow the input activity. Example, for a DELAY of 6, the CRT will show a flat baseline for about 200 ms (6 x 32.8 ms) during the delay. The signal from the entire input cycle will then be flashed on the screen for 32.8 ms as the readout scan takes place. The digital outputs, however, hold the output magnitude reading from one scan to the next. Because of the update rate mentioned in the previous paragraph, the numeric display updates may appear irregularly when a non-zero delay setting is used.

4.4D EXTENDED DELAY ACCESSORY

When the Model 1207 Extended Delay Accessory is installed and activated, selecting the REAL TIME mode disables the extended delay function. This allows the use of the normal real time mode to set up certain of the 1207 functions.

4.4E PLOT/PRINT

Except as noted in the next subsection, the PLOT/PRINT mode is not normally usable in the REAL TIME mode. Unless the printer or plotter can handle 500 five-digit channels in 32.8 ms, the output for each channel will be the result of a different scan. In general the preferred approach is to print or plot the results of a PRESET = 1 memory accumulation.

4.4F SINGLE CHANNEL VS TIME PLOT

The REAL TIME mode may be used in conjunction with the PLOT/PRINT mode to plot the output of one channel as a function of time. The channel advance is disabled by setting the PLOT RATE (rear panel) to Ø or by use of the cursor remote program buss PGMLN12B1 (see Section IX — INTERFACING). The PLOT/PRINT control then activates the plotter sweep and the output will follow the cursor-selected channel.

This mode may also be used with a printer if the data rates are compatible. This may be achieved in several ways: (1) use of a fast printer; (2) use of an appropriate DELAY setting to reduce the data rate; (3) use of the DATAREQDØ — DATAREADYD1 control lines (see Section IX — INTERFACING) to hold the outputs stable until the printer completes its cycle.

4.5 OPTICAL INPUT ALIGNMENT

Four basic input conditions affect the performance of the OMA Detector: focus, dispersion of the input for each channel over the entire 0.2" x 0.001" signal portion of the channel element, alignment of the input signal element with the detector channel element, and the presence of signal light on the "dark" or subtracting half of the detector target area. In many cases the input format will allow the necessary alignment to be performed using the OMA's REAL TIME mode and CRT display.

> **NOTE**
>
> The figures in this section are idealized sketches intended to illustrate specific operating characteristics. Actual operation of the instrument may not duplicate the figures. However, the desired adjustment is normally readily identified by the "peaking" or optimization of the characteristic indicated in the figure.

4.5A FOCUS

The input image must be focused on the detector target plane, and not on the vidicon faceplate. A defocused image results in light spreading onto adjacent channel elements, and appears as a rounding of sharp intensity level transitions on the CRT display. For example, the CRT peak

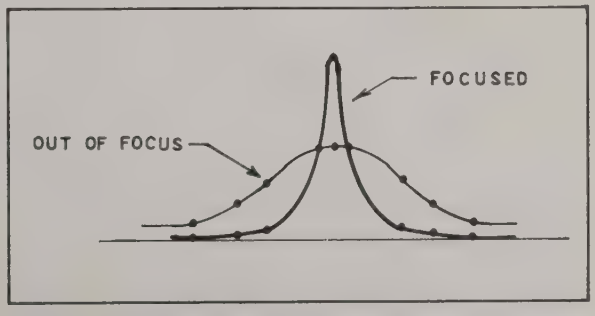


Figure IV-4. FOCUSED AND NON-FOCUSED SPECTRAL LINES

representing a defocused spectral line will be lower and spread over more channels, but will have the same integrated area as that of a focused line.

4.5B DISPERSION OVER CHANNEL ELEMENT

Under "normal usage condition", the input light for each channel should be dispersed over the full 0.2 inch height of the 0.2 x 0.001 inch detector element (e.g., a 0.2 inch high slit image from a spectrometer). If the input light is imaged as a point on the detector element, local saturation of that point may occur while using only a fraction of the light integrating capability of the entire detector element.

The maximum usable input signal level is limited by the dynamic range of the electronics, and any potential input overload condition is detected and indicated by the O.M.A. error light (in the numeric display window). However, local saturation of a point within a channel element may not raise the total signal level for that channel to a level which will activate this indicator.

4.5C ALIGNMENT OF CHANNEL ELEMENT

The 0.2 x 0.001 inch signal for each channel must be aligned with the corresponding detector element. Rotational misalignment (e.g., spectrometer slit not perpendicular to grating dispersion and detector frame scan) causes each channel's input to be spread over several detector elements. On the CRT display this causes an effect similar to a defocused image.

If the input signal extends beyond the 0.2 inch height of the detector channel element, it will either extend into the subtraction or "dark" half of the detector, or into a region where the light will not be detected but will represent a potential source of scattered light within the instrument.

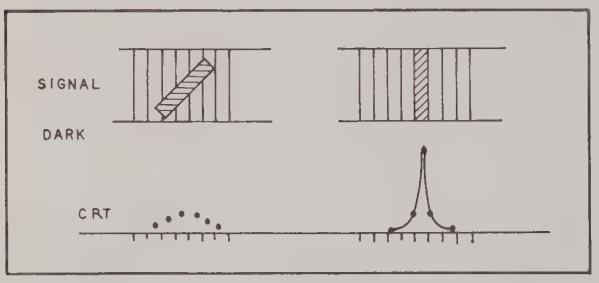


Figure IV-5. EFFECT OF ROTATIONAL MISALIGNMENT

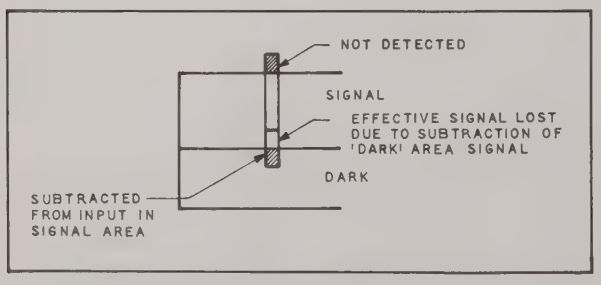

NOT DETECTED
SIGNAL
EFFECTIVE SIGNAL LOST DUE TO SUBTRACTION OF 'DARK' AREA SIGNAL
DARK
SUBTRACTED FROM INPUT IN SIGNAL AREA

Figure IV-6. EFFECT OF SIGNAL EXTENDING BEYOND DETECTOR SIGNAL CHANNEL ELEMENT AREA

4.5D SIGNAL LIGHT IN "DARK" AREA

Each detector channel element consists of a 0.2 x 0.001 inch signal element and a corresponding 0.2 x 0.001 inch element in the "dark" area of the detector. The "dark" element is used to compensate for vidicon dark current and for stray light on the detector. Any signal light which falls on this region is subtracted from the signal on the corresponding "signal" area. A negative excursion on the CRT display, particularly one just following an intensity peak, is indicative of signal light on the "dark" area.

Note that the dark area is not normally intended for signal subtraction, and, in order to optimize signal dynamic range, the O.M.A. console provides only limited dynamic range for "negative light" ("dark" input in excess of "signal" input). If balanced operation is desired, the O.M.A. console must be recalibrated for "400 mode" operation (see Section VI – CALIBRATION).

4.5E DETECTOR ASSEMBLY ROTATION

Rotation of the detector assembly with respect to an otherwise correct input image produces a combination of the above effects. For example, consider a spectrometer imaging spectral lines normally on channels 10, 250, and 490. Due to the detector assembly rotation, all three channels are misaligned. This spreads the signal into adjacent channels in an apparent defocusing effect. The channel 250 peak is simply rotated and thus loses amplitude but retains the same total area. The channel 10 peak has some of its signal displaced into the non-scanned region, and shows a loss of amplitude and integrated signal area. The channel 490 peak has some of its signal displaced into the subtraction region ("dark area"), and thus shows twice the loss of integrated signal. Because of the channel rotation, some of the channel 490 signal appears as a negative excursion in the preceding channels.

Note that the alignment of the channel element is much more critical than alignment of the 500-channel input with the frame scan direction. If the detector head is rotated approximately 1/2 degree from the optimum setting, a single channel input will be rotated over two detector channels, halving the per-channel signal. The error due to the ends of a channel element being rotated off of the signal area will be less than 1% (worst case, channels 0 to 499). If necessary, this latter effect can be eliminated by

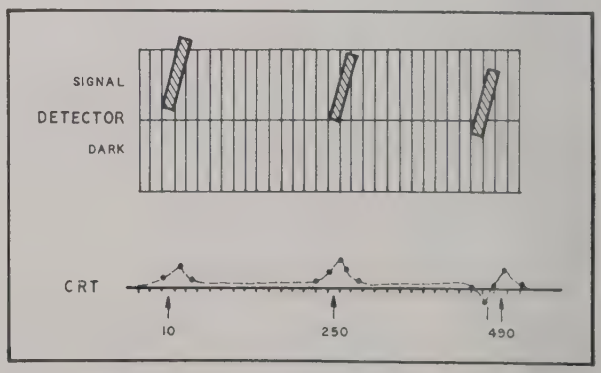


Figure IV-7. DETECTOR ASSEMBLY ROTATION

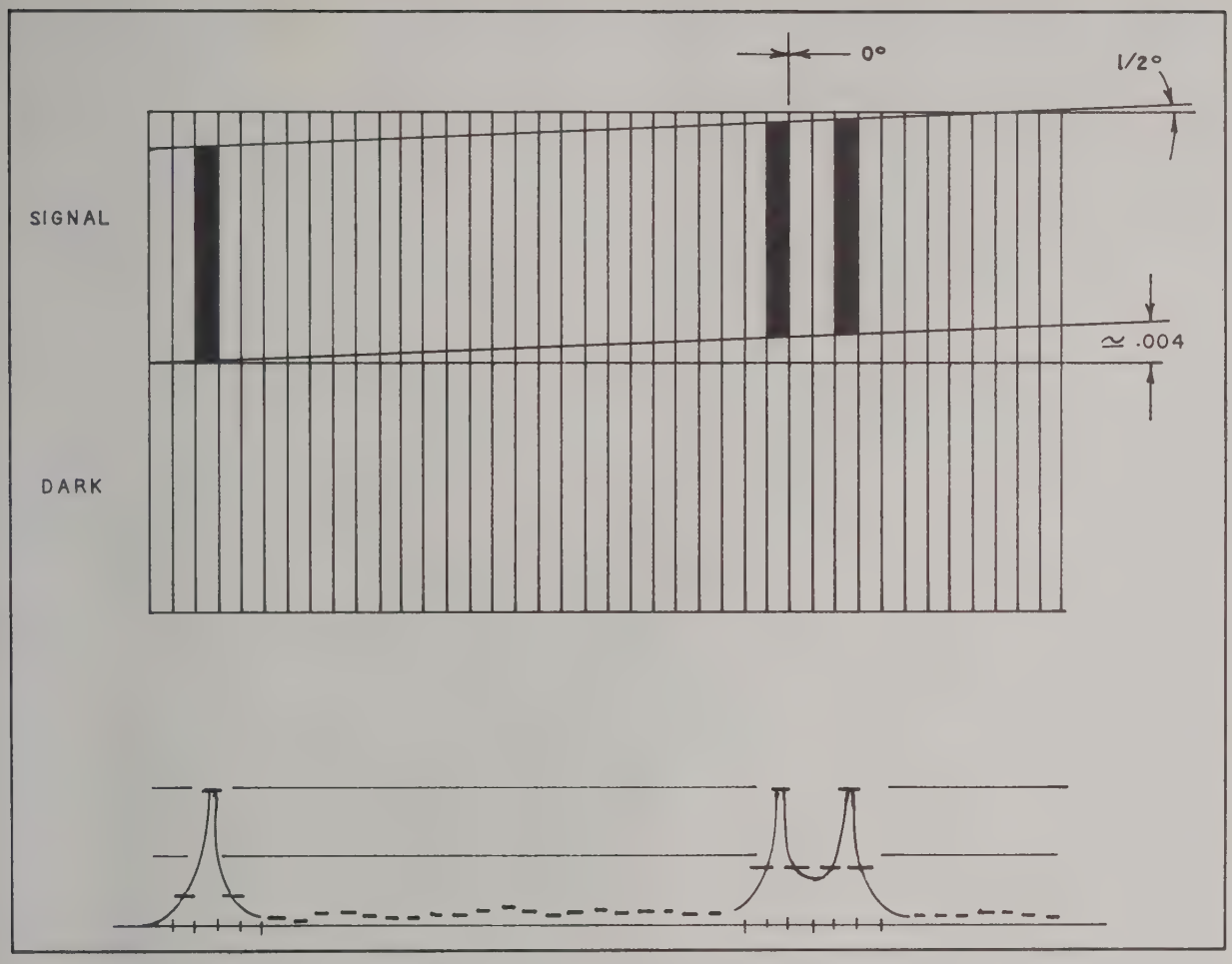


Figure IV-8. SLIT VS GRATING MISALIGNMENT

reducing the length of the input signal element to eliminate the light falling on non-signal areas.

Consider a spectrometer with 1/2 degree of error in the alignment of the slit with the grating (Figure IV-8). The Detector Head would normally be rotated to align the detector channel elements with the slit image, in order to optimize spectral resolution. The nonlinearity resulting from the misalignment between the spectral dispersion and the frame scan direction would be eliminated by a 2% reduction in effective detector area.

4.5F ADJUSTMENT TECHNIQUE

The following procedure assumes that the detector head electronics are properly adjusted as shipped from the factory (see Section VIII), and that the detector head has been mounted in approximately the correct position.

(1) Set the O.M.A. console to observe the REAL TIME CRT display (press REAL TIME, set SCALE FACTOR = 10^3, DELAY = 0, TEST pushbutton released, both DISPLAY EXPAND controls in CAL position).

(2) Apply an input signal, such as a spectral line, that will result in a sharp contrast line between two detector channels.

(3) Adjust the input light level so that some kind of response is observed on the CRT display when the light is turned on and off, or when the input image is moved to a different channel. The input level should not be so great as to cause the error light to light up in the console's numeric display window.

(4) If the CRT display baseline goes negative, or limits at −100 when the light input is applied, it indicates light on the "dark" portion of the detector. Check that the detector board has not been mounted upside down, and adjust the input image in a direction that will move it onto the "signal" area. It is not necessary to optimize this adjustment at this time, but a positive going signal should be obtained.

(5) Adjust the optical focus and detector head rotation for optimum output. Each of these adjustments has an optimum position which will result in a minimum number of channels in the spectral peak or contrast

transition. In the case of a spectral line type of input, this will also result in maximum peak height. These two adjustments are independent, but it will be difficult to observe the optimum setting of either if the other is severely misadjusted. Thus both adjustments should be touched up until no further improvement is observed.

(6) Focus and alignment may bring the peak channel input up to the input overload level (indicated by the error light in the numeric display window). Reduce the input light level as necessary to prevent this condition.

(7) Displace the input image into the "dark" region of the detector, indicated by a loss of signal amplitude on the CRT display. Adjust the input image back toward the "signal" area, observing the increasing magnitudes on the CRT display. Stop this adjustment at the point where no further magnitude increase is noted. Continued adjustment would cause the magnitudes to fall off again as a portion of the input image is displaced into the non-signal area.

(8) Optical and camera tube crosstalk will spread some of the signal from a single channel area into the adjacent channels. Consider a single channel input such as a spectral line image of a 25 micron slit, focused and aligned on a single channel detector element. Because the crosstalk spreads some signal into the adjacent channel on either side, the number of channels in the peak cannot be reduced to less than three. Slight rotation or focus errors appear as extra crosstalk rather than as extra channels in the peak. The final adjustment of focus and rotation is for minimum apparent crosstalk; i.e., maximum center channel magnitude and minimum side channel magnitude.

(9) Unlike the focus adjustment, detector head rotation displaces the image slightly in the channel number direction. This can split the input signal between two channels. For the final rotation adjustment, proceed as follows.

(a) Note the center channel peak magnitude in the numeric display window.

(b) Rotate the detector head very slightly.

(c) Readjust the image in the channel number direction to center the input image on one channel.

(d) Check the new peak reading for possible improvement.

(10) Repeat the adjustment in step 7 with input signal on a number of channels from 000 to 499. The required

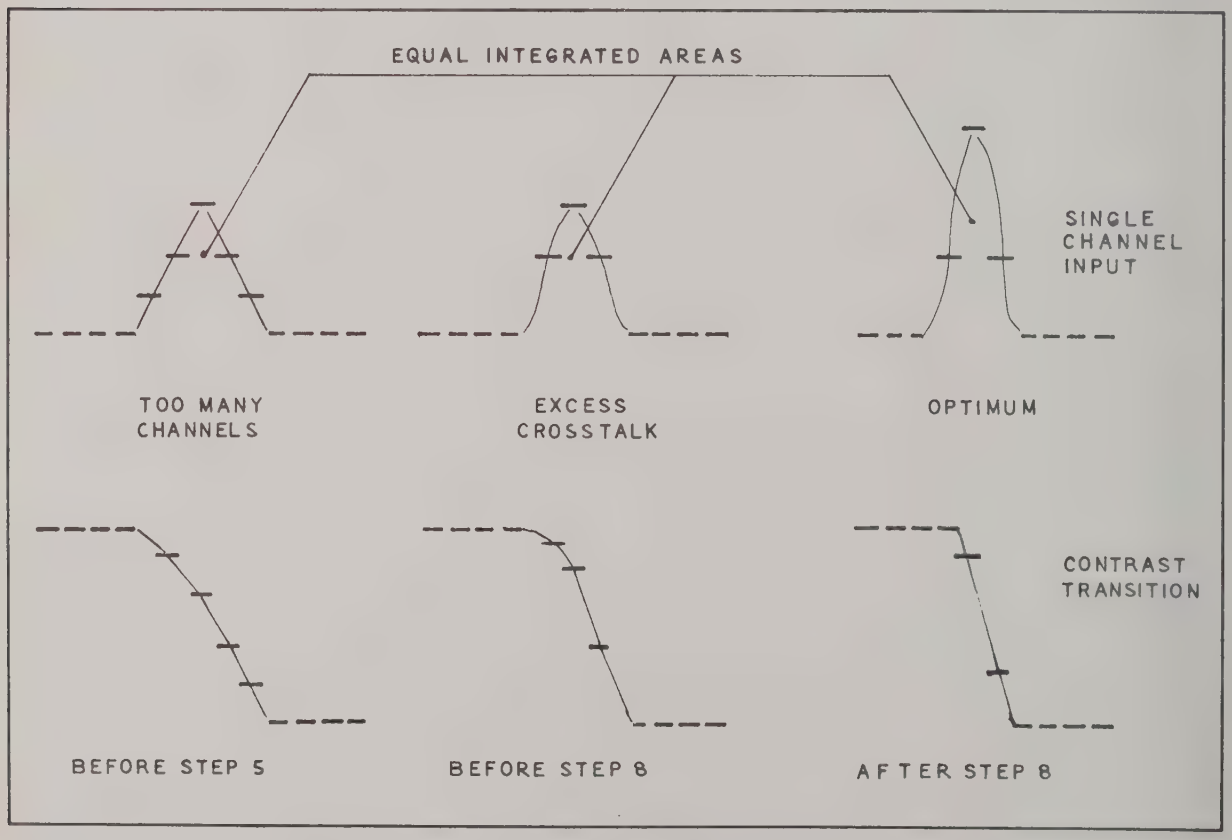


Figure IV-9. CROSSTALK

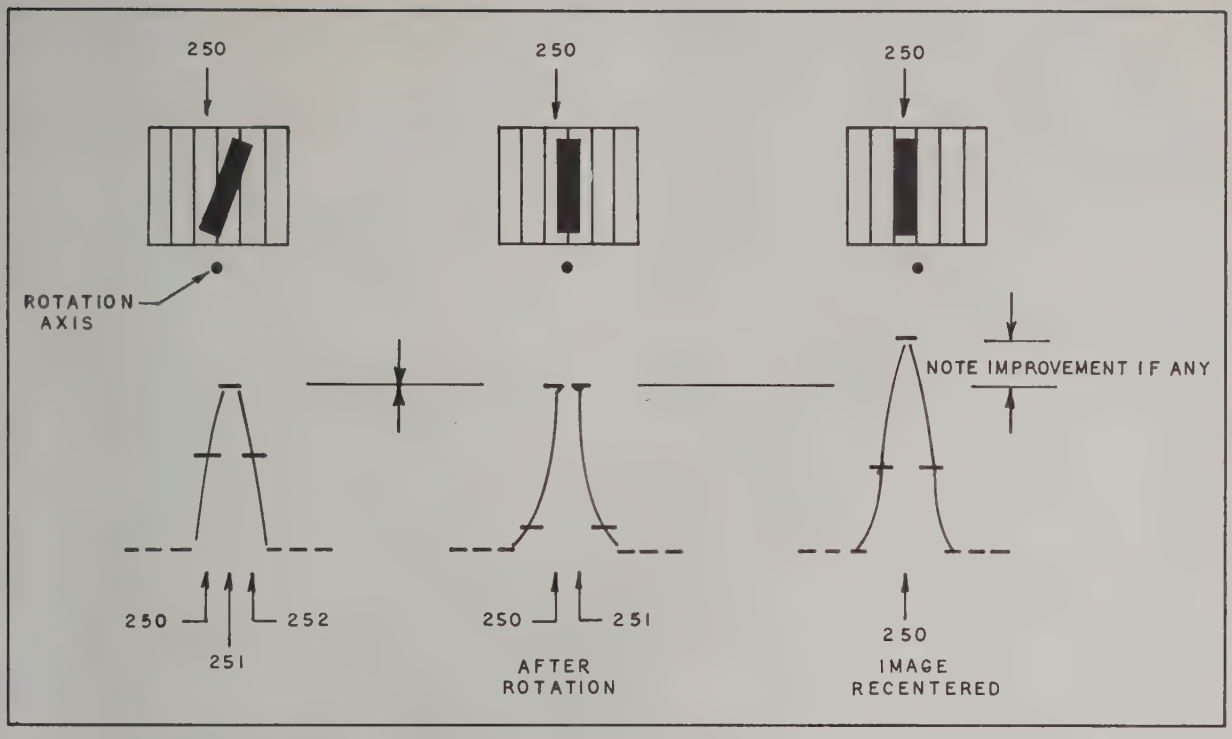


Figure IV-10. DETECTOR HEAD ROTATION

setting of this adjustment should be the same for all channels. If not, refer to Subsection 4.5E.

4.6 INPUT CONSIDERATIONS

4.6A INPUT OVERLOAD

The O.M.A. is designed so that, under normal operating conditions, the maximum input signal per channel will be limited by the characteristics of the A-D Converter in the O.M.A. console. This allows the input overload condition to be detected and indicated before it adversely affects the measurements.

An error light in the numeric display window indicates when the input level for any channel reaches 732 counts. The instrument is linear at this point, and remains linear to 783 counts (7% overrange) in the REAL TIME mode or 860 counts/scan (17% overrange) during memory accumulation. (The difference is due to difference in the digital timing.) The input light level should normally be adjusted so that the error light is off, in order to assure linear operation of the O.M.A.

Three input overload conditions which are not detected and indicated by the error light and which are caused by incorrect instrument setup are:

(1) Excess light on the "dark" half of the vidicon, causing a "negative signal" limit condition. This appears as a baseline at −100 on the CRT and numeric displays. See Subsection 4.5D.

(2) Local saturation of the vidicon due to the input signal being imaged as a point on the vidicon. This appears as a signal peak which responds to input light up to, but not over, some level, that level being less than the normal saturation point. See Subsection 4.5B.

(3) Preamplifier saturation due to excessive integration delay. This appears as a positive or negative baseline which does not respond properly to changes in input light level. See Subsection 4.6B.

4.6B INTEGRATION DELAY

The vidicon target integrates the light falling upon it between one scan and the next. Increasing the delay between successive scans (DELAY $>$ Ø) can improve the signal-to-noise ratio of low-level signals and improve the ability to read the signal out in a given number of scans.

Naturally, the preferred approach is to have enough input light to provide near limit signal levels in the peak channels with DELAY = Ø. However, when signal levels are low, an integration delay may be used, so long as the input overload condition is not reached.

The ability to use a given integration delay is limited by the dark current of the vidicon target, and thus by the operating temperature of the vidicon. The dark current and the signal current are both integrated during the integration delay. A scan beam chopping technique compensates for the effects of dark current. However, residual difference between the light and dark halves of the vidicon target result in baseline variations. This effect increases with

integration delay, and will use up part of the available input dynamic range. In addition, the dark current will eventually saturate the scan beam chopping circuits. This is the third effect mentioned in Subsection 4.6A.

In practice, if the REAL TIME display is observed as the DELAY setting is increased, a point of diminishing returns will be observed. At room temperature this usually turns out to be at about DELAY = 4. Since the dark current is reduced at reduced temperatures, cooling the detector allows the use of longer delays.

4.6C TARGET LAG

The ability of a single vidicon scan to read out the light signal integrated on a target element is related to the signal and dark current levels. Although the O.M.A. can detect picosecond light pulses, several 32.8 ms scans may be required to completely read the signal from a low-intensity flash. This effect also appears as a slowed response to changes in signal level when the signal levels are very low, or when the vidicon is cooled to reduce dark current. The effect is therefore referred to as target lag.

Because of target lag, it is difficult to eliminate the effect of input events occurring just before the start of a memory accumulation. If such effects represent a potential problem, they should be eliminated by an appropriately synchronized shutter or by gating of the intensifier stage of the 1205D Detector assembly.

4.6D CHANNEL SKEW

Each vidicon target channel element integrates light for the entire interval from one scan of that element to the next, and each target element is active for the same total amount of time. However, since the channels are scanned sequentially, the time interval seen by each channel differs from that of the adjacent channel by 64 μs. Thus the measurement interval seen by channel ØØØ always starts and stops exactly 32 ms before that of channel 499.

The channel skew is associated with starting and stopping the scanning process. It is constant for any single continuous memory accumulation regardless of the number of input cycles or the integration delay setting used. A 100 second memory accumulation would require 100.032 seconds to complete, and all but the first and last 32 ms would be common to all 500 channels.

Within a single input cycle (or in the REAL TIME mode), the twelve-channel (768 μs) vidicon retrace interval and any integration delay are common to all 500 channels of that input cycle. This is the interval from the completion of the previous scan of channel 499 to the beginning (at channel ØØØ) of the scan for the current input cycle.

The effect of channel skew is most apparent if the light signal is turned on or off at some random time during the input cycle. If the light signal is turned on and left on, all 500 channels will see the light start at the same time, but at the end of the measurement channel ØØØ will "stop looking" 32 ms before channel 499. If the light were evenly distributed over the 500 channels, the channel skew would appear as a ramp on top of the accumulated signal, with channel 499 indicating 32 ms more signal than channel ØØØ (Figure IV-11). The slope of this ramp is entirely determined by the magnitude of the signal step, and is unaffected by the DELAY setting, the total signal accumulated, or the phase relationship between the signal transition and the scan cycle.

Note that if the signal light is turned off during the measurement, the net effect is that channel ØØØ starts 32 ms before channel 499, and they all end at the same time when the light is turned off (Figure IV-12). This produces a ramp effect exactly opposite to the effect of turning the same signal on. Thus the two effects are neatly cancelled if the signal light is turned on *and* off during the same measurement. In fact, the error caused by this effect is determined by the difference between the signal levels at the beginning and end of the measurement. Any number of changes in signal level may occur during the measurement without introducing any additional error.

4.6E SKEW LAG EFFECT

A second order effect is caused by the combination of channel skew and target lag. If the light signal is turned both on and off during the measurement (as in the case of a flash input), all channels will see the same amount of input light. However, after the light is turned off, some channels will receive one more readout scan than the rest, due to channel skew. Because of the target lag, the light signal on these channels will be more completely read out into the memory.

The effect of this is most noticeable when the target lag is large, i.e., when signal levels are very low, or when the vidicon dark current is reduced by cooling.

Since the error is caused by the increment in completeness of signal readout associated with the extra scan of the later channels, it may be minimized by allowing the O.M.A. to continue scanning for a short interval after the end of the flash. Even in this relatively difficult low light level example, the signal increment for one extra scan is very small after 20 scans.

The skew lag effect is eliminated if the flash occurs entirely within the frame retrace interval or during a DELAY interval, thereby avoiding the channel skew. This is the reason for recommending the flash synchronizing technique detailed in Subsection 4.6G.

4.6F SIGNAL TIMING

The operation characteristics mentioned in the preceding subsection result in the following order of preference for the various available signal timing methods.

(1) The light signal is turned on before the measurement commences, and remains on until after the O.M.A. measurement cycle is completed. This category includes applications involving a continuous stream of short duration flashes, with a large number of flashes during each scan interval.

(2) A flash event is synchronized with the O.M.A. cycles so that the entire event, or each intensity transition in

the event, occurs entirely within a frame retrace or DELAY blank interval (see Subsection 4.6G).

(3) The light signal is turned on after the O.M.A. measurement begins, and is turned off at least one scan before the measurement cycle ends. An application of the O.M.A. remote program capability (Subsection 4.6H) allows the measurement cycle to be synchronized with the external light signal control to insure this condition. The skew-lag effect will be minimized by allowing up to 20 or more additional scans after turning off the light.

(4) Random signal timing. In this condition, the skew and lag effects are minimized if the number of accumulation cycles is large, or, for a given number of accumulation cycles, if the signal intensity is large.

4.6G TRIGGERING FLASH PHENOMENA

As mentioned in the previous subsection, the skew and lag problems can be eliminated for flash-type events if they are synchronized with the O.M.A. cycle. This technique is based on the assumption that the flash mechanism of interest can be triggered by an output that is derived from the 1205A console.

Figure IV-11 is a schematic representation of the O.M.A. timing for a measurement with a preset hold after three scan cycles. Some of the signals available at the rear panel REMOTE PROGRAM connector are also shown. Note that in each input cycle, there is a retrace interval following the scan of channel 499 (for the previous cycle) and before the scan of channel ØØØ (at the beginning of the current cycle). This is the interval noted in input cycle C, the first active input cycle in Figure IV-11. This interval is common to all 500 channels for scan C, and thus any flash event occurring entirely during this interval will be free of skew and skew-lag effects.

Figure IV-12 expands the interval of interest for scan C. There is no signal conveniently available to mark the exact beginning of the desired interval. However, each of the three signals shown provide a leading edge transition which marks the beginning of a 600 μs portion of the flash time. The flash event should be synchronized to occur during this interval.

(1) Single Flash

The DELINHD1 signal is recommended for synchronizing single flash measurements. (Note that all of these outputs should be buffered to meet the requirements specified in Section IX – INTERFACING.) If the flash is triggered by the negative-going transition of this signal, a single synchronized flash will occur at the beginning of the measurement, as shown in Figure IV-11. Although the example shown indicates a preset hold after 3 scans, signal-to-noise is usually optimized by 10 to 20 readout scans. For background subtraction purposes, the DELINHD1 signal may be combined with the AACCUMSWDØ signal so that the flash will only be triggered for an "A" memory accumulation.

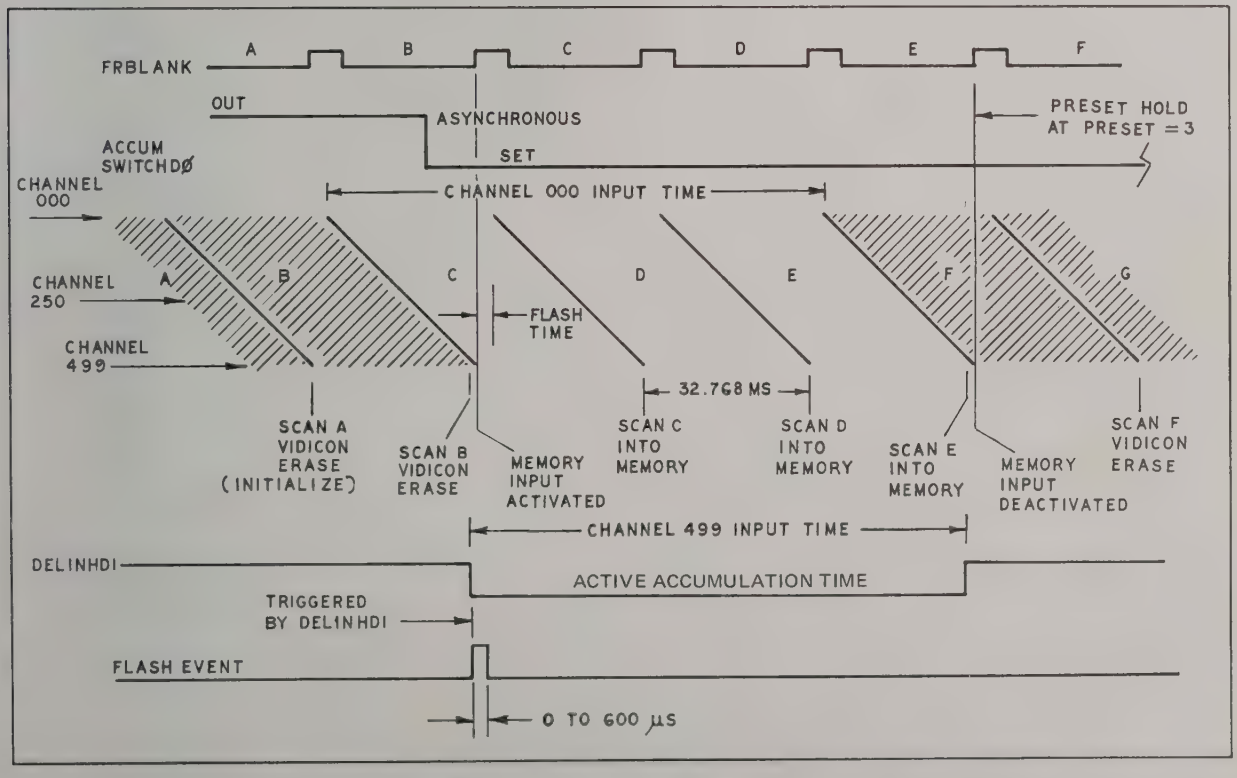


Figure IV-11. FLASH SYNCHRONIZATION

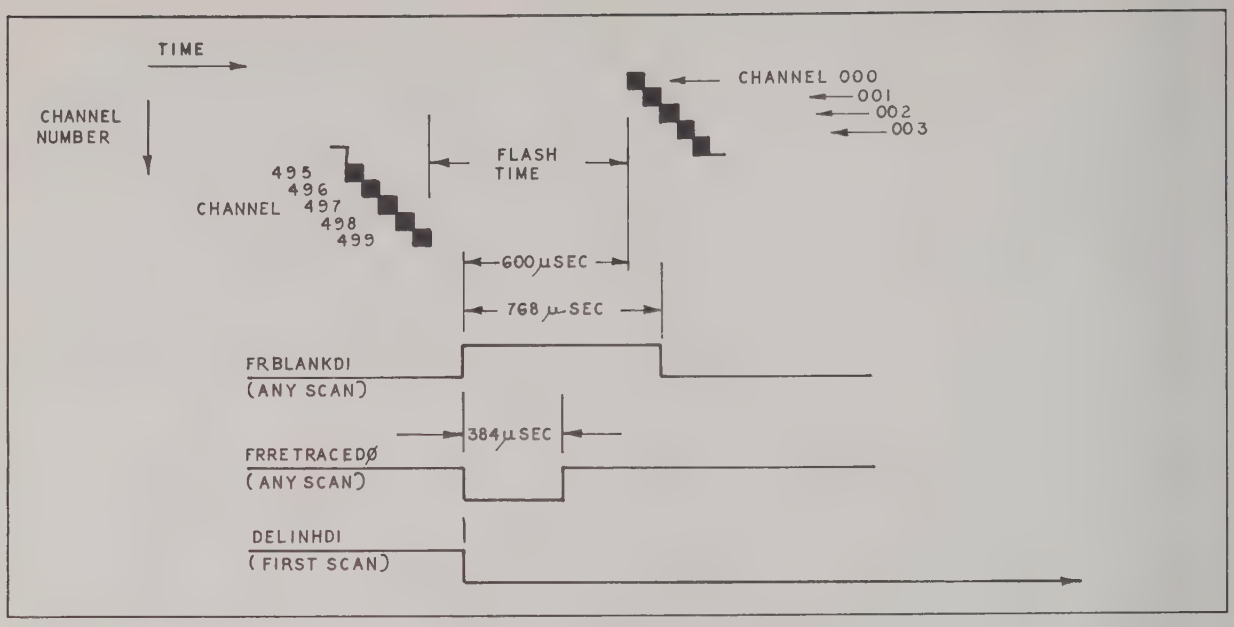


Figure IV-12. FLASH INTERVAL, EXPANDED

(2) Multiple Flash

The frame blank signal FRBLANKD1 and the frame retrace signal FRRETRACEDØ mark the flash interval as shown in Figure IV-12 for every 32.768 ms cycle, whether accumulation is taking place or not. These signals may therefore be used to synchronize multiple flashes for viewing in the real time mode, or for multiple-flash measurements. An external counter may be used if necessary to trigger the flash at some sub-multiple of the frame rate. FRRETRACEDØ is shorter than the available flash time, and is therefore a useful gating signal if the flash is shorter than 384 μs.

(3) Slow Flash

If the flash duration is greater than 600 μs, the integration delay may be used to extend the usable flash time. A DELAY setting of 1, for example, would provide 32.768 ms of additional flash time in each input cycle. The input overload and integration delay requirements mentioned in Subsection 4.6A and 4.6B must be considered when this mode is used.

The FRBLANKD1 and FRRETRACEDØ signals are not changed by the DELAY setting. If multiple flashes are to be observed, external circuitry will be required to locate the flash interval by counting FRRETRACEDØ pulses. The measurement will always start with the DELAY interval, so the single flash synch. technique may be used. However, the accumulated background signal associated with the extra readout scans will be increased, since there will be an additional delay interval for each extra scan.

The optimum measurement for single slow flashes makes use of an external circuit to control the O.M.A. integration delay function to provide a delay in the first input cycle of the measurement, followed by continuous scans for optimum readout. Figure IV-13 shows an example of this application.

4.6H MEASUREMENT PRETRIGGER

The technique described below makes use of the particular characteristics of the MEMORY ERASE mode to allow the instrument to record events which start slightly *before* the O.M.A. measurement cycle is activated.

In normal operation, the timing of the input cycle results in a delay of up to 32 ms from the asynchronous activation of the ACCUM control to the time when all 500 channels are active. Figure IV-14 shows an example of a typical manually controlled measurement. The same results would be achieved with a preset hold at PRESET = 3. Note that the measurement begins with the first input cycle, with a readout scan that starts after the ACCUM control is activated. If the control is activated just after an erasing scan is begun, i.e., at channel ØØØ time of erase scan B, 32 ms will elapse before all 500 channels will be integrating the signal for transfer into memory.

Figure IV-15 shows the technique under discussion. Both the ACCUM control and the corresponding MEMORY ERASE control are activated at some time prior to interval of interest. The memory erase mode erases each channel just before the next scan of that channel takes place. As in the case of the ACCUM mode, the timing is such that either all or none of the 500 channels are erased during a given cycle. While both controls are active, the effect observed on the CRT display appears the same as the REAL TIME mode. That is, at any given time, the CRT displays the results of a single input cycle. (Figure IV-15 scan A and scan B.) However, unlike the REAL TIME mode, the results

of each scan are saved for 32 ms before being erased from the memory.

When the beginning of the interval of interest is detected, the MEMORY ERASE control is released. The effect is that at the beginning of the next scan *the results of the previous scan are not erased.* The current scan is added to the previous scan, and the effect is that the measurement started with the scan prior to the release of the MEMORY ERASE control.

Compare Figure IV-14 with Figure IV-15. Note that the activating control transition (A ACCUM or A MEMORY ERASE) occurs during the same time window in both examples. However, the measurement controlled by MEMORY ERASE in Figure IV-15 starts one ACCUM CYCLE earlier than that of Figure IV-14.

The MEMORY ERASE control also continuously resets the PRESET HOLD counter. Thus, if both measurements were terminated by the PRESET HOLD mode at PRESET = 3, both would have the same total measurement time. The Figure IV-15 measurement would start and stop 32.768 ms before Figure IV-14, ending after scan D. Input cycle E would not be included in the memory erase measurement.

The memory erase controls may be operated via the rear-panel REMOTE PROGRAM inputs AMEMERSWDØ

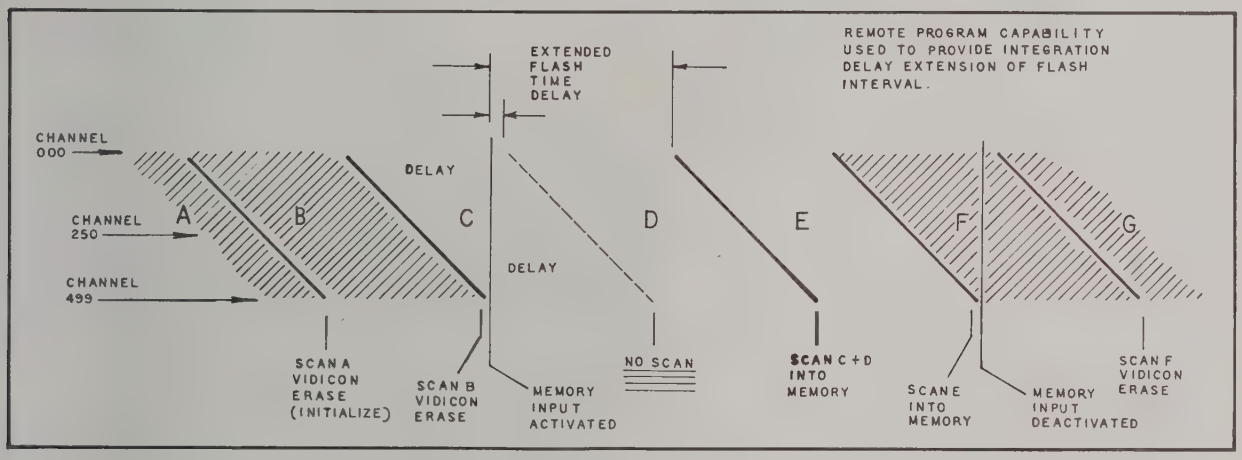


Figure IV-13. REMOTE PROGRAM CAPABILITY

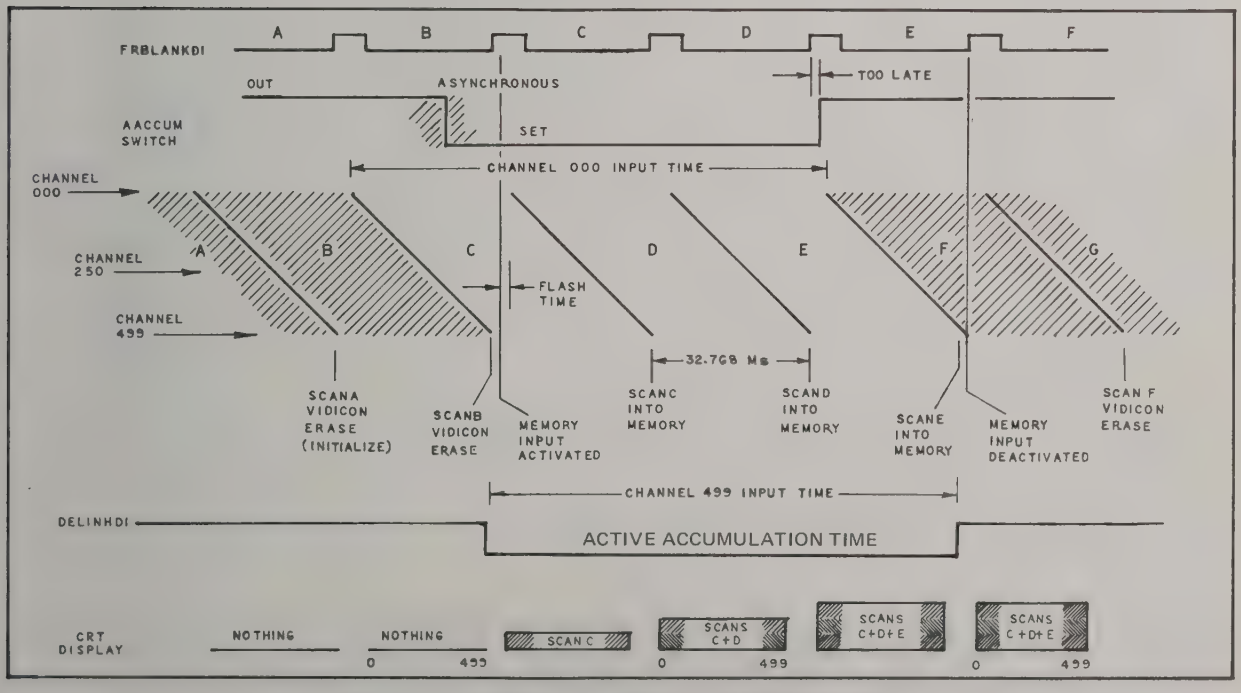


Figure IV-14. MANUALLY CONTROLLED MEASUREMENT

and BMEMERSWDØ. This allows the measurement to be triggered by a signal from the external experiment, or by evaluating the output from each channel (except 499) in the PSEUDO-REAL TIME output and activating the measurement when the desired results are observed. The MEMORY ERASE control may be released up to 100 μs after the event of interest begins, or at any time prior to the next positive-going transition of FRBLANKD1.

Since each application of this technique erases the results of any previous experiment, it is not possible to accumulate several measurements into memory.

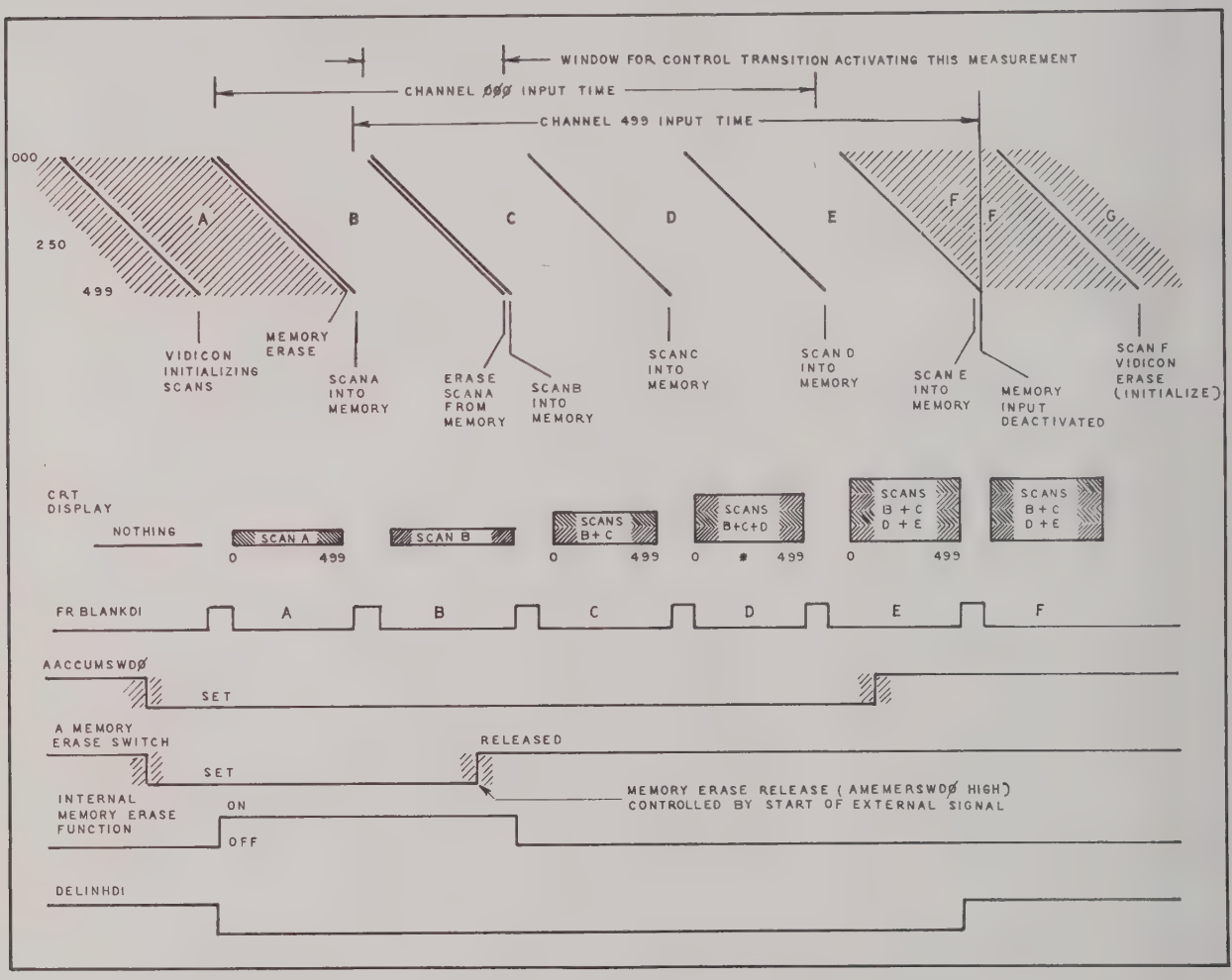


Figure IV-15. MEMORY ERASE CONTROLLED MEASUREMENT

SECTION V
OPTIONS AND ACCESSORIES

5.1 MODEL 1205D SIT DETECTOR HEAD

5.1A DESCRIPTION

The Model 1205D Detector consists of a silicon intensified target camera tube (SIT), deflection components, high voltage power supply, and preamplifier. This detector head is compatible with all standard 1205A consoles and is designed to be interchangeable with the standard 1205B silicon vidicon detector head. Although the 1205D has the same cross section and mounting geometry as the 1205B, it has an increased length. Contact P.A.R.C. for updated or detailed information regarding this option.

The primary advantage of the 1205D over the 1205B is an improvement in sensitivity in the visible and UV spectral regions. This improvement is due to the use of an electron image intensifier section ahead of the target section of the tube. Since the silicon target and preamplifier are essentially the same for the 1205B and D, the dark current noise, preamplifier noise, and signal processing are also the same. The factor by which the 1205D sensitivity is improved is thus a function of the intensifier electron gain and the quantum efficiency ratio of the SIT photosurface (S-20) and of the silicon vidicon photosurface.

$$\text{1205D S/N GAIN} = \frac{G_e\ (\text{q.e.})\ \text{SIT}}{(\text{q.e.})\ \text{SV}}$$

With an electron gain of 1500 and a quantum efficiency ratio of 0.2 (for the visible region), the 1205D will have a S/N gain of 300 in comparison to the 1205B. For signals strong enough to be seen with the REAL TIME CRT display, the quantum noise due to the signal photoelectrons will limit the 1205D S/N. Thus, the formula for the S/N gain above is only true for the weak signal case. For either type of noise, signal averaging will improve the S/N ratio in proportion to the square root of the accumulation time.

For wavelengths greater than 850 nm, the S-20 quantum efficiency is less than 0.07 percent and the S/N gain for the SIT is less than unity. Thus, for wavelengths between 850 nm and 1100 nm, the 1205B will provide higher S/N.

For wavelengths less than 350 nm, the 1205D can be supplied with a fluorescent film over the fiber optics faceplate of the SIT which will convert UV photons into visible region photons. The overall quantum efficiency for this type of converter film is one to two percent (ratio of photoelectrons from the S-20 photocathode to input UV photons). Response of films of this type is generally flat down to X-ray wavelengths. Since the film can be very thin, resolution will not be impaired, and since it is transparent in the visible and near IR, it need not be removed for measurements in these spectral regions.

Because of pincushion distortion in the intensifier section of the SIT, there will be a loss of resolution and sensitivity at high and low channel numbers. To minimize this effect, the line scan for the 1205D is readjusted in amplitude and position. For some spectroscopy applications, the reduced image size of the 1205D will cause a loss of system sensitivity. In these cases, a full size (1205D) scan format may be used with the realization that sacrifice will be required for resolution and uniformity in the frame scan (channel number) direction. For cases where lag or dark current are important system parameters, the scan dimensions and the illuminated area on the faceplate should be minimized.

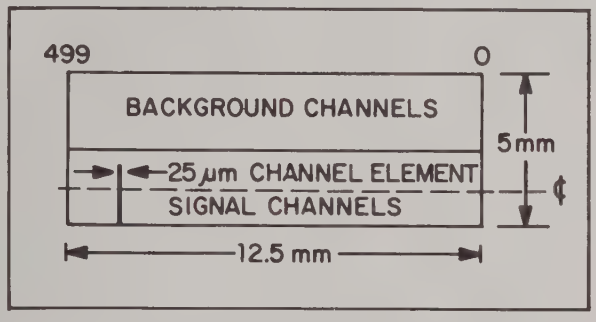


Figure V-1. FACEPLATE IMAGE FORMAT FOR MODEL 1205D (NEGATIVE GATING)

The intensifier of the 1205D SIT provides a convenient gain control capability through changes in photocathode (accelerating) voltage. A range of 2 kV to 9 kV for photocathode voltage provides electron gains ranging from 1 to 1500. For best focus at widely differing gains, the 1205D will require rotational readjustment about its axis.

Although the 1205D can be gated through control of the photocathode-to-target voltage (9 kV), it can also be gated by controlling the voltage between the photocathode and the intensifier focus electrode. The gating voltage in this case is 12 percent of the full accelerating voltage. With the SIT normally on, it can be gated off by applying positive going pulses at the MHV input at the rear of the 1205D.

The SIT can be biased off by switching the photocathode to a more positive voltage on the high voltage bleeder string at the front of the SIT. This can be done with a toggle switch accessible through a threaded plug near the front of the 1205D. With this switch in the forward position, the SIT is normally off, and it can be gated on with negative going pulses at the MHV gating input.

To preserve the intensifier focus in the gated mode, stable, flat-topped gating pulses with sharp rise and fall times are required. Gate pulse durations can range from 10 ns to 2 ms, limited at the short end by photocathode resistivity, and at the long end by a time constant in the high voltage bleeder chain.

To avoid gate pulse interference in the preamp and 1205A video processor, it is desirable to gate while the vidicon is not scanning (reading beam blanked). For pulse durations up to 800 μs and pulse repetition rates of 30 Hz or less, the

gating might be performed within the frame scan retrace interval. Using the delayed accumulation mode, gating pulses during the delay intervals will not cause interference. A variety of pulse generators suitable for gating of the 1205D are available commercially. In general, when gating the SIT, the skew, lag, and flash timing considerations (SECTION IV) will apply. If a terminating resistor is used, it should be placed outside the 1205D Housing. Since some Model 1205D Detectors have positive gating to turn the SIT on, the SIT can be turned off by a negative pulse at the MHV input with the toggle switch set to NORMAL. The SIT can be turned on by a positive pulse at the MHV connector with the toggle switch set to GATE. Further information may be obtained from Princeton Applied Research Corporation.

5.1B 1205D PRECAUTIONS

(1) Do not allow strong light on the SIT faceplate when the high voltage is on.

(2) Do not touch the SIT faceplate or insulating regions near the front of the tube.

(3) High voltages are present at both the front and rear of the 1205D whenever the 1205A console is on and connected.

(4) If the connection between the 1205A and D is broken while the 1205A is on, high voltages will remain within the 1205D.

(5) Do not allow the SIT photocathode voltage to exceed –9 kV.

(6) Damage to the SIT may result from excessive vibration, shock, or positioning of the tube with faceplate end down.

(7) Turn the power off before handling the gating mode control toggle switch.

5.1C TEST AND ADJUSTMENT

The test and adjustment procedure for the 1205D is the same as the 1205B with the following exceptions:

(1) Intensifier high voltage adjustment.

(2) Gating circuitry test.

(3) Readjustment of line scan amplitude and position.

> **CAUTION**
>
> Although the SIT tube in the 1205D Housing can withstand moderate room light for short periods of time with a low photocathode voltage, it is advisable to have the 1205D connected to a polychromator before the 1205A is turned on.

5.1D INTENSIFIER HIGH VOLTAGE

Before adjustment of the 1205A as described in the instruction manual, the high voltage adjustment potentiometer in the 1205D Housing should be adjusted so that 3 V rms (9 volts pk-pk) appears at the testpoint (TP-1) on the high voltage power supply board. This will result in a photocathode voltage of 2.9 kV, as shown in Figure V-2. The sensitivity of the 1205D will now be approximately the same as the 1205B in the visible spectral region.

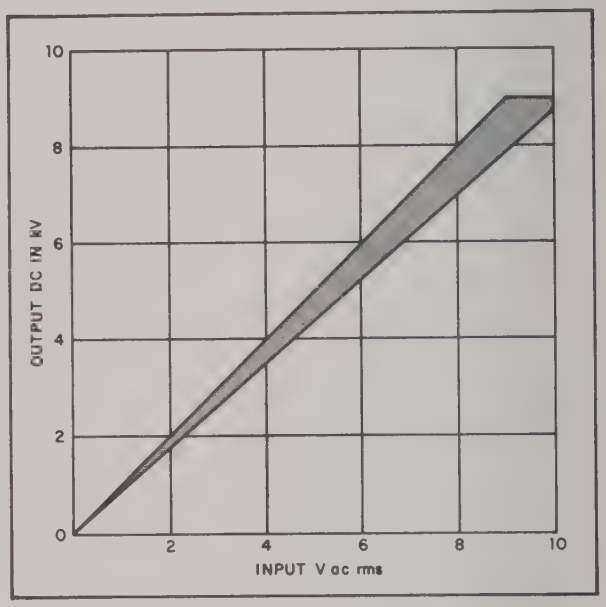


Figure V-2. PHOTOCATHODE VOLTAGE AS A FUNCTION OF INPUT AC VOLTAGE

The checkout and test procedure as described for the 1205A/B may now be performed using the same polychromator/optics setup as is normally used.

After completion of the 1205A adjustments, proper operation of the 1205D may be verified by changing the intensifier high voltage and observing the effect on sensitivity and noise. Increasing the high voltage from 2.9 kV to 4.0 kV (using the high voltage adjustment potentiometer) should result in an improvement in sensitivity by a factor of ten. Increasing from 4.0 kV to 7.2 kV should provide another factor of ten improvement, and increasing from 7.2 kV to 9.0 kV should provide another factor of 1.5 improvement. Rotational readjustment of the 1205D Detector assembly with respect to the polychromator will be necessary to maintain focus whenever the photocathode voltage is changed.

With no light on the SIT faceplate, the random noise observed on the CRT display will increase by less than a factor of 1.5 with a photocathode voltage change from 0 to 9.0 kV.

5.1E LINE SCAN AMPLITUDE AND POSITION READJUSTMENT

To maximize uniformity of response and resolution as a function of channel number, the 1205D line-scan amplitude should be reduced and the line scan repositioned. The amplitude should be reduced to 1/2 the normal ac voltage on TP-1 of the Line Scan card (4.1 V pk-pk or 2.2 V rms). With switch S1 on the Line Scan card in the ADJ position,

the L. POSN potentiometer should be adjusted to provide +0.50 V dc offset on TP-1 of the Line Scan card. The line-scan voltage waveform should now display zero-crossing transients 1/4 of the distance between rising and falling edges of the waveform rather than 1/2 of the distance as is the case for the 1205B.

5.1F GATING

General

The 1205D, as normally supplied, accepts negative going gating pulses (some earlier models are wired for positive gating) which are capacitively coupled to the photocathode. A pulse amplitude of 1100 to 1300 volts is required for best focus when the 1205D is operated at full gain. Smaller pulse amplitude will suffice for reduced gain (accelerating potential) setting.

Required Equipment

In addition to the 1205D, a high-voltage pulse source, such as the P.A.R.C. Model 1210 or Velonex 340 and an interconnecting cable, such as the P.A.R.C. Model 6020-0302-14 is required. Velonex 340's supplied by P.A.R.C. will include the proper plug-in (type 2189) for interfacing to the 1205D. The connector for the HV pulse is a type MHV. The Velonex type 340 requires an external pulse generator capable of producing 10-15 V pulses across the 100 Ω input impedance of the Velonex 340. The generator determines the width, delay, and repetition rate of the gating pulses. The delay of the 340 is less than 500 ns if the rise time of the driving pulse is 10 ns or less. The Velonex duty factor may not exceed 1%. Its rise time is 50 ns.

The P.A.R.C. Model 1210 pulse generator contains integral pulse width and pulse delay controls. It can be triggered by pulses having amplitudes from +1 V to +10 V (TTL levels will trigger it) and may be remotely programmed for pulse width and delay. The M1210 provides up to 50% duty factor, and can gate either positive-gated or negative-gated 1205D's by changing internal switch settings. The rise time is 2 μs.

Operation

With the 1205A power off, unscrew the plastic plug at the front of the 1205D and set the miniature toggle switch located under it to the gated position. Then replace the plug. Connect the HV pulse generator to the 1205D using the MHV cable. If a 1210 is used, adjust the delay and pulse width to place the gate in the desired time relationship to the experiment. Focus is achieved by varying the pulse amplitude. If the experiment does not lend itself to adjusting the focus during the experiment, drive the pulse generator at the same pulse width and repetition rate as will be used in the experiment, and use a known light source for adjustment of the focus. If a Velonex 340 is used, it will be necessary to use an external pulse generator with pulse-width and pulse-delay controls to adjust the time relationship of the gate.

Coupling Time Constant

The gating pulse is RC coupled to the SIT with a time constant of 200 ms. Consequently droop and defocusing will occur on longer pulses. The Model 1210 incorporates a droop compensation circuit for pulses up to 100 ms.

5.2 1205K SERIES HOUSING

5.2A DESCRIPTION

The Dry Ice Cooled Housing can be used to provide cooled operation of the 1205KB detector, the 1205KD detector, the IR enhanced 1205KE detector, or the UV sensitive 1205KF and 1205KG detectors. Cooled operation of these detectors provides increased sensitivity for steady-state light sources. The improved S/N ratio is achieved because of the reduction in the vidicon dark current, since the dark current decreases by a factor of 10 for each 25°C, exposure times of up to 3000 seconds (50 min) can be used.

The Dry Ice Cooled Housing accommodates the vidicon tube, deflection coil assembly, and electronic filter networks for the vidicon electrode voltages. "O" ring seals provide a moisture tight compartment which is shielded electromagnetically to reduce interference. A thermopane window provides a totally frost-free optical path. The cold period for a maximum load of dry ice is about 10 hours after initial cool down. Once loaded with dry ice, operation can be maintained in any position without loss of coolant or degradation of performance.

5.2B COOLED DETECTOR HEAD PERFORMANCE

Cooling a silicon vidicon tube to −70°C reduces the dark-current portion of the charge on the silicon target by a factor of 10^4. This allows the target to be exposed to a light source for at least a factor of 10^4 longer than an uncooled silicon vidicon target before dark-current noise limiting occurs.

5.2C SIGNAL-TO-NOISE IMPROVEMENT

As a result of cooling the target to near dry-ice temperatures, an improvement in signal-to-noise of 10^2 (square root of 10^4) over that obtainable with an uncooled detector head is possible by exposing 10^4 times longer with the cooled detector head. The longer exposure time results from the factor of 10^4 reduction in dark current that occurs in cooled operation.

5.2D EXPOSURE TIME - 1205A O.M.A.

Up to 999 frame scan delay intervals (32.8 ms each) can be obtained for a total of approximately 328 seconds by setting the S1 and S2 mode switches of the PRESET card (in the O.M.A.) to the left-hand position.

With the addition of the Model 1207 Extended Delay Accessory, exposure times of up to 2-3/4 hours can be obtained. Refer to Subsection 5.3 for discussion of the Model 1207 Extended Delay Accessory.

5.2E COOLED HOUSING FEATURES

The cooled housing has several features incorporated in its design such as a dial thermometer, a hermetically sealed inner chamber, a thermal insulating window, a No-Dew heater ring, LED flash diode, and provisions for adapting to a light source. Refer to the Interface Control Drawing

9680-C-MD for the location of these features on the cooled housing. A brief description of each follows.

(1) Dial Thermometer: The dial thermometer allows the temperature of the vidicon target to be read directly in degrees centigrade after the dry-ice has been allowed to cool the housing for one hour.

(2) Airtight Sealed Vidicon Chamber: The vidicon tube is installed in an inner chamber sealed with an O-ring to prevent frost from building up on the vidicon tube envelope.

(3) Thermal Insulating Entrance Window: A double pane insulating optical window serves as a thermal insulator to prevent frosting of any part of the window. The window is pyrex glass for 1205KB and 1205KE Series Detector Heads. In the case of a 1205KF, KG or KD Detector Head, a quartz window is used for UV enhancement.

(4) No-Dew Heater: The entrance window has a No-Dew heater ring around the window to prevent formation of condensation on the outer window surface. This feature provides an optically clear light path to the vidicon image plane. The heater requires 6 V dc at 500 mA. Connection is made through a BNC connector at the rear of the Housing.

(5) LED Flash Diode: Refer to Subsection 5.4A on the Model 1207 Extended Delay Accessory for the function of the LED.

(6) Light Source Adapter: The Cooled Housing should be mounted on a base plate using the mounting holes provided.

5.2F SPECIFICATIONS

(1) Operational:

(a) Tube target operating temperature: $-76^{\circ}C, \pm 1^{\circ}C$ stability over an ambient range of $0^{\circ}C$ to $+40^{\circ}C$.

(b) Limiting ambient temperature for 12 hour operation is $30^{\circ}C$. Maximum ambient without damage to equipment is $70^{\circ}C$.

(c) Coolant: Crushed dry-ice (1/2" chunks).

(d) Cooling period - 12 hours maximum when loaded with 1/2" chunks of dry-ice to a line even with the top of the silver-colored metal ice reservoir.

(2) Mechanical:

(a) Size: 10-1/4" wide x 12-1/2" high x 12-5/16" long (26 cm x 31.8 cm x 31.2 cm).

(b) Weight: 17 pounds (7.7 kg) with coolant [16 pounds (7.3 kg) less coolant].

(c) Mounting: Face mounted via four (4) holes on front and four (4) holes on bottom of cooled housing.

5.2G ACCESSORY

A manual ice-crusher is supplied with the 1205K Series Housing.

5.3 MODEL 1207 EXTENDED DELAY ACCESSORY

5.3A DESCRIPTION

The Model 1207 Extended Delay Accessory expands certain functions of the Model 1205 Optical Multichannel Analyzer for applications involving a cooled vidicon. It provides extended vidicon signal integration delays of 1 to 9999 seconds duration (1 sec to 2-3/4 hours). One to eleven vidicon scans per delay interval may be selected as required for complete signal readout. The maximum usable delay will depend on the detector target.

A feature of the Extended Delay Accessory allows modification of the vidicon beam potential during the scan interval to achieve signal readout with minimal conversion noise. An automatic cycle then resets the vidicon with a short flash of light and recharges the vidicon target to the correct potential for signal integration. Provision is made for light biasing as an alternative vidicon conditioning method.

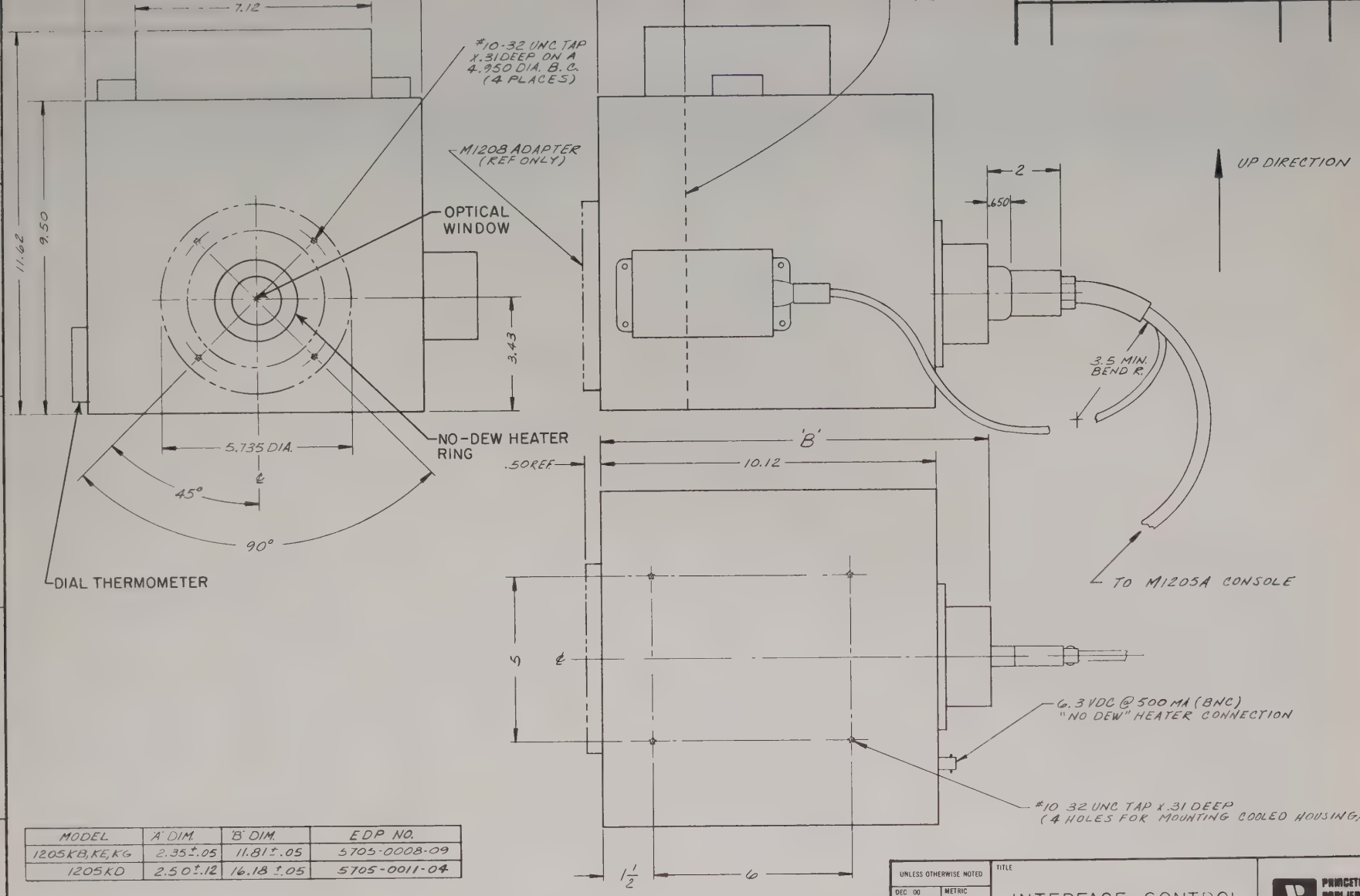
The vidicon filament may be switched off automatically during all but the last 20 seconds of long delay intervals, and provision is made for interruption or premature termination of the delay cycle. All operations are synchronized with the normal O.M.A. timing sequence, allowing multiple input cycles using the O.M.A.'s PRESET and FULL SCALE hold modes. All 1207 functions may be externally controlled via the REMOTE PROGRAM connector.

5.3B INSTALLATION

The Model 1205A Console must be factory modified to accept the Extended Delay Accessory. This modification consists of a new clock crystal and installation of the necessary signal and power connections to the Model 1205A AUXILIARY connector.

5.3C SPECIFICATIONS

Delay Time: 1 s to 9999 s
Vidicon Scans: 1 to 11 scans per delay cycle
Reset Flash: 12 mA to 100 mA LED current sink, duration 33 ms to 330 ms
Recharge Scans: 2 to ≈20 after each reset flash (adjustable)
Vidicon Target Voltage Increment: 0 to 1000 mV (0 to −1 V)
Auto Filament: Filament off during all but the last 20 seconds of delay intervals
Light Bias: 10 μA to 3 mA LED current sink during the erase scans of a non-accumulate interval



MODEL	'A' DIM.	'B' DIM.	EDP NO.
1205KB,KE,KG	2.35±.05	11.81±.05	5705-0008-09
1205KD	2.50±.12	16.18±.05	5705-0011-04

UNLESS OTHERWISE NOTED	
DEC 00 ·01	METRIC
DEC 000 ·005	FRAC ±1/64
SCALE 1/2 x 1	ANG ±1/2°
DRWN E.J.B	DATE 4-7-75
CHKD	4-7-75
APPD	4-9-75

TITLE: INTERFACE CONTROL DWG.

PRINCETON APPLIED RESEARCH

MODEL NO. 1205 KB,KD,KE,KG

PRINCETON APPLIED RESEARCH CORPORATION
P.O. BOX 2565
PRINCETON, N. J. 08540

PART NO. SEE TABLE

DWG. NO. 9680 C-MD SHT 1 of 1

REV — SHT — OF — DWG NO 9680-C-MD

5.4 MODIFICATION OF THE MODEL 1205A O.M.A. FOR USE WITH THE MODEL 1207 EXTENDED DELAY ACCESSORY

5.4A DESCRIPTION

This modification allows certain 1205A functions to be expanded for applications involving cooled vidicon detector heads (Models 1205KB, 1205KD, 1205KE, and 1205KG). The modification provides the 1205A with the following features when used with the 1207.

(1) Extended vidicon signal integration delays of 1 to 9999 seconds duration (1 second to 2-3/4 hours).

(2) One-to-eleven vidicon scans per delay interval as required for the complete signal readout.

(3) Modification of the vidicon beam potential cathode voltage during the vidicon scan interval to achieve optimum signal readout with minimal conversation noise.

(4) An automatic reset for the vidicon target by means of a flash of light from a flash lamp or a light-emitting diode (LED). The flash recharges the vidicon target to the correct potential for signal integration.

(5) Provision for an alternative method of conditioning the vidicon by means of light biasing.

(6) Automatic switching of the vidicon filament voltage OFF during all but the last 20 seconds for long delay intervals.

(7) Provision for interruption or premature termination of the delay interval.

All operations are synchronized with the normal 1205A O.M.A. timing sequence, allowing multiple delay interval cycles using the O.M.A.'s PRESET and FULL SCALE HOLD modes.

The 1205A O.M.A. operates normally, even if modified for use with the 1207, provided it is *not* connected to the 1207 through the interface cable or, if connected, provided the 1207 power is OFF. It also operates normally when connected to the 1207 with the O.M.A. operated in the REAL TIME mode.

5.4B MODIFICATION

The actual modification, which is factory-installed and included in the price of the Model 1207, consists of a new clock crystal, along with the necessary signal and power connections to the AUXILIARY connector at the 1205A rear panel. The wiring list for the AUXILIARY connector follows.

Pin No.	Signal Name
1	FRRETRACE DØ
1 SHIELD	GROUND
2	NO PIN INSTALLED (N.C.)
3	+5 V SUPPLY (O.M.A. +5 V)
4	–15 V SUPPLY
5	GROUND
6	AACCUMSW DØ
7	NO PIN INSTALLED
7 SHIELD	
8	BACCUMSW DØ
9	DELINH D1
10	DELBLANK 2DØ
11	PRECLOCK 2DØ
12	FILON A–
13	VCATH AN
13 SHIELD	GROUND
14	SDELAY DØ
15	REALSW DØ

Table V-1. 1205A TO 1207 AUXILIARY CONNECTOR (AUX) WIRING LIST

5.5 MODELS 1205F AND G, UV AND QUARTZ DETECTOR HEADS

The Model 1205F UV Detector Head and Model 1205G Quartz Faceplate Detector Head are identical to the standard Model 1205B Detector Head with the exception of the vidicon detector used. Both of these special silicon vidicon tubes provide better UV response and differ only in the amount of additional response. Figure V-4 shows the basic difference between the Detector Heads. Contact P.A.R.C. for updated or detailed information regarding these options.

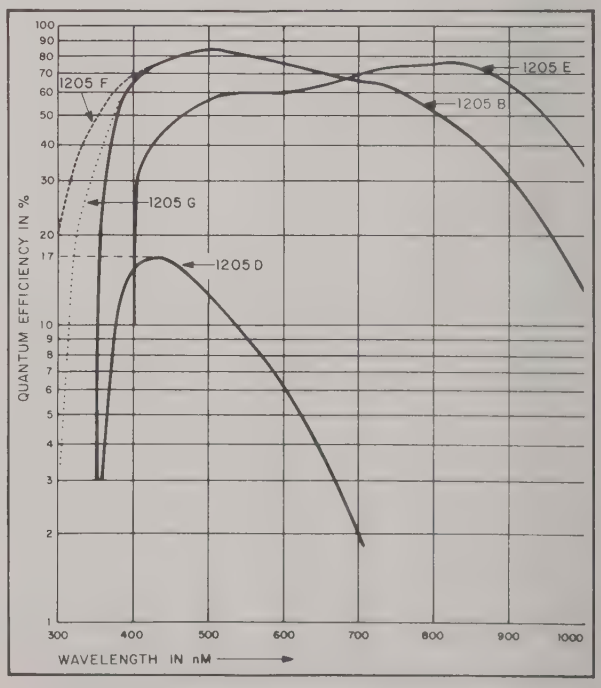


Figure V-4. DETECTOR HEAD SPECTRAL RESPONSE

The vidicon used in the Model 1205G Quartz Faceplate Detector Head is the same as the standard vidicon except for the Quartz window. This vidicon provides better UV response and retains the same response as the standard tube from 400 nm to 1100 nm.

The vidicon used in the Model 1205F UV Detector Head has a specially processed target as well as a Quartz faceplate for even better UV response. Due to the thin target used in this vidicon, the response above 700 nm is not quite as good as the standard detector.

5.6 MODEL 1205E IR ENHANCED DETECTOR HEAD

The Model 1205E IR Detector Head is identical to the 1205B, F, and G detector heads except the IR response from 700 to 1200 nm is enhanced. The 1205E target is thicker for improved absorption of light in this region, and the target is anti-reflection coated to minimize moire interference in this region. The improved sensitivity and uniformity above 700 nm makes this the best 1205 series detector for measurements in this region.

5.7 SERIAL CONVERTER, OPTION -03

5.7A DESCRIPTION

The Serial Converter Option allows data to be transmitted to a teletype or other serial printer, a communications line, a time-shared computer, some tape recorders and tape punches, or other character-serial digital devices. Outputs are available in 8 bit USASCII format, either serial-by-character or serial-by-bit. Four-bit BCD character-serial bit-parallel output is available from the four low-order USASCII bits. The data rate may be set to match the output device.

The output data format consists of 6 character words, each followed by a separator. The first word is an identification word giving the source (A memory, B memory, Difference or Accumulate Cycles) and memory address for the data which immediately follows. The next five words are data. Each data word consists of a negative sign character for negative data and 5 numeric characters (leading zeros are suppressed). Every sixth word is followed by a carriage return and a line feed. See Table V-2 for a TYPICAL O.M.A. PRINT OUT.

5.7B SPECIFICATIONS

Output Format: Two to six hundred words per readout. There are two types of six-character words, identification words and data words.

Identification words have the following characters:

1 & 2 ----- Source Identifier: A (for the A memory), B (for the B memory), D (for the Difference between the A & B memories, A–B), AC (for A accumulation cycles), BC (for B accumulation cycles), and DC (for A–B accumulation cycles). Single character identifiers are followed by a space.

A	Ø	131	–32	2	12Ø	–65
A	5	54	7	–74	19	41
A	1Ø	–6Ø	126	–89	–24	129
B	15	Ø	Ø	Ø	Ø	Ø
B	2Ø	Ø	Ø	Ø	Ø	Ø
B	25	Ø	–27	–85	124	–61
D	3Ø	45	14	–74	12	5Ø
D	35	–64	122	1	–32	131
AC	4Ø	–42	1	1	1	1
AC	45	1	1	1	1	1
AC	5Ø	1	Ø	Ø	Ø	Ø
BC	55	Ø	Ø	Ø	Ø	Ø
BC	6Ø	Ø	Ø	Ø	Ø	Ø
BC	65	Ø	1	1	1	1
DC	7Ø	1	1	1	1	1
DC	75	1	1	1	1	1
DC	8Ø	1	1	1	1	7
A	85	1589	6981	9132	11472	13730
A	9Ø	15585	20094	22544	24690	26955
A	95	16294	33416	35583	21309	39997
A	1ØØ	42353	46388	48931	51170	53325
A	1Ø5	55549	60052	61960	64420	66673
A	11Ø	38208	73170	75420	77580	79830
B	115	81990	86400	88650	90810	92970
B	12Ø	95220	99630	1790	4040	6200
B	125	8450	12860	–274	51	–41

Table V-2. TYPICAL O.M.A. PRINTOUT

3 ----- Space

4, 5 & 6 ----- Memory Address

Data words have the following characters.

1 ----- "—" sign for negative data, a space for positive.

2, 3, 4, 5 & 6 ----- A five-digit number (leading zeros are suppressed, the minus sign is located just ahead of the first digit).

Normally, six words are considered to be a block. Each word is followed by the separators. A normal block consists of the following.

1. An identification word
2. Two-space characters
3. A data word
4. Three spaces
5. A data word
6. Three spaces
7. A data word
8. Three spaces
9. A data word
10. Three spaces
11. A data word
12. A carriage return and a line feed

It should be noted that the address in the identification word is for the first data word. The next data word is from the next consecutive address.

Data Rate: 50 to 125,000 characters per second, preset, for bit-parallel output. 5 to 720 characters per second, preset, for bit-serial output.

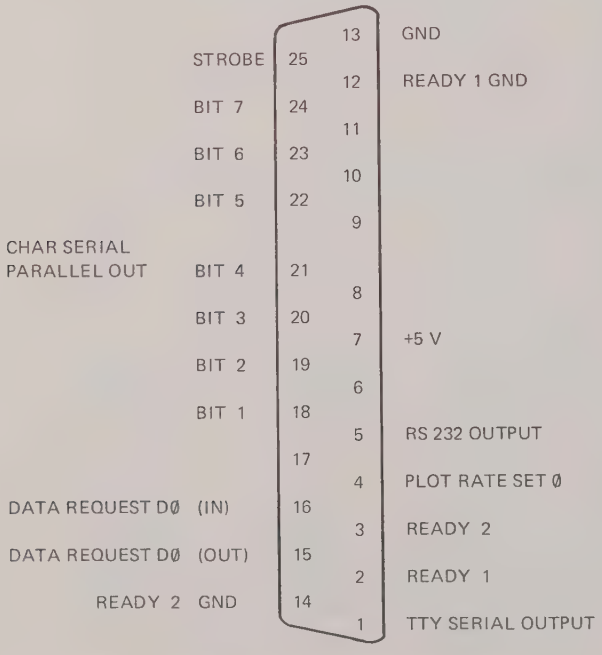


Table V-3. SERIAL OUTPUT CONNECTOR PINOUT

Serial Output: Asynchronous, 11 bit sequence (1 start bit, 8 information bits, 2 stop bits).

Synchronous, full dialog with external equipment with one word per dialog. Dialog is achieved by using the READY 1 or READY 2 line. This line goes high to request data from the serial converter and must remain high until the start bit or the data ready pulse is received. This line must go low again before the last character is out, to prevent the output of the next word.

20 mA "TTY battery" positive current source provided.

"1" = "mark" = TTL low, "0" = "space" = TTL high.

An RS232 output is also provided.

Parallel Output: 8 bit lines, 1 data-ready line. TTL levels, up to 12 mA sink. The bit lines are active high, and the data-ready line is active low.

The data-ready (strobe) pulse is 9% of the character duration. An inverted strobe is available on the card.

5.7C INSTALLATION

Introduction

This option is normally considered a factory installation. The output from this option is available on the back panel of the 1205A console (SERIAL OUTPUT connector). The Serial Converter Card is plugged into Slot #12 of the mother board.

Installation with Teletype Model 33

Operation of the serial converter with a Model 33 Teletype requires the use of the P.A.R.C. interconnecting cable, Model 110382 (part #6020-0382-01). The Model 33 Teletype must be wired for a 20 mA loop current. This should be done as follows:

(1) Check that terminal strip #151411 inside Model 33 is wired thus:

Terminal	Wire Color
1	White
1	White
2	Black
2	Black
3	Gray
3	White/Red
4	Red
4	Orange/Green
5	White/Blue
5	Brown/Yellow
6	White/Black
6	White/Yellow
7	Red/Green
7	White/Brown
8	Black/Green
9	Yellow
9	Violet

(2) Connect pin 1 of the 25 pin input connector of the TT 33 (the connector into which the 110382 cable will be plugged) to terminal 6 of the terminal strip 151411. This wire carries serial data from the O.M.A. Connect pin 7 of the input connector to terminal 7 of terminal strip 151411 (+5 V from O.M.A.).

(3) Check that the large green power resistor (181816), located on the right side middle of the teletype, is wired as follows.

Terminal	Wire Color
1	White/Green
1	White/Green
2	Green
2	Green
3	—
4	Blue

Installation with Facit Punch, Model 4070

Operation of the serial converter with a Model 4070 paper punch requires the use of a P.A.R.C. Model 110383 cable (part #6020-0383-02). If the user desires, the serial converter data may be set at the factory to take advantage of the higher data rate capability of the 4070, compared to the teletype. However, the 4070 may also be operated at low speed, if it's desired to use the same serial converter card with both devices. The Model 4070 must be set up for parallel data entry in accordance with the manufacturer's instructions. Model 4070's supplied by P.A.R.C. will normally be so adjusted.

5.7D OPERATION AND MODIFICATIONS

Introduction

The serial converter option is normally used to obtain a hard copy output of data in the 1205A memory which is the result of some experiment. Assuming such data have been accumulated into the memory, one selects the display mode desired to display the data (A, B, A–B, Accum Cycles, etc.), sets the PLOT RATE switch (thumbwheel, rear panel of 1205A) to zero, turns on the output device (teletype should be set to LINE), sets the CURSOR of the 1205A to channel 0, and presses PLOT/PRINT. The serial converter will automatically advance the cursor through all 500 channels of the 1205A memory and cause the data stored there to be printed by the output device.

Modifications to -03 Option

(1) The -03 option may be modified to conserve output medium by printing a more compact output format. The compact format starts with a source identifier and the channel number corresponding to the first data word. The rest of the output contains only data and spaces, with no subsequent carriage return, line feed, source identifier, or channel numbers. This is most often used with the paper punch. This is done by cutting the ribbon to I.C. 11 pin 6 (74LS54) and grounding pin 1 of I.C. 14. This may be done as either a factory or field modification. If done as a field modification, this should be indicated on the board itself and on the exterior of the 1205A, in case the unit should be returned for service.

(2) Even or odd parity of the parity check bit may be selected by connecting a jumper between E5 and E6 (odd parity) or between E7 and E8 (even parity).

(3) Input threshold levels at READY 1 and READY 2 are typically +2 V and –2 V for logic 1 and 0 respectively. These may be shifted to +2.1 V and +1.0 V (typical) by installing jumpers between points E1 and E2 for READY 1, and between E3 and E4 for READY 2.

Console Modifications

The necessary console wiring changes for the -03 option are normally done by the factory, and are listed below for reference only.

(1) JUMPERS INSTALLED

Connector 5 Pin 41 to Connector 12 Pin 36 (BSEDØ)
Connector 5 Pin 40 to Connector 12 Pin 34 (ASWDØ)
Connector 8 Pin 31 to Connector 12 Pin 37 (ACCUMCYSW DØ)
Connector 8 Pin 29 to Connector 12 Pin 29 (SLOMODE D1)
Connector 8 Pin E to Connector 12 Pin E (DATA READY D1)
Connector 8 Pin E to Connector 12 Pin 27 (LNADVCLK DØ)

(2) SERIAL OUTPUT CONNECTOR (see Table V-3)

Pin 1 to Connector 12 Pin 31 (TTY Serial Out)
Pin 2 to Connector 12 Pin 9 (Ready 1)
Pin 3 to Connector 12 Pin 11 (Ready 2)
Pin 4 to Connector Terminal C of Plot/Rate switch on rear panel
Pin 5 to Connector 12 Pin 30 (RS232 Out)
Pin 7 to Connector 12 Pin 2 (+5)
Pin 12 to Connector 12 Pin 10 (Ready 1 GND)
Pin 13 to Connector 12 Pin 1 (GND)
Pin 14 to Connector 12 Pin 12 (Ready 2 GND)
Pin 15 to Connector 12 Pin 8 Data Req. DØ (Out)
Pin 16 to Connector 8 Pin J Data Req. DØ (In)
Pin 18 to Connector 12 Pin 39 (Bit 1)
Pin 19 to Connector 12 Pin 40 (Bit 2)
Pin 20 to Connector 12 Pin 41 (Bit 3)
Pin 21 to Connector 12 Pin 42 (Bit 4)
Pin 22 to Connector 12 Pin 38 (Bit 5)
Pin 23 to Connector 12 Pin 33 (Bit 6)
Pin 24 to Connector 12 Pin 32 (Bit 7)
Pin 25 to Connector 12 Pin 43 (Strobe)

5.8 DUAL HEAD CARD SET, OPTION -05

This is a set of three cards that eliminates most readjustments when switching detector heads. When two detector heads are to be used with the 1205A console, a second set of cards eliminates the necessity for readjusting the electronic focus and alignment controls. The Dual Head Card set consists of a HIGH VOLTAGE card, a LINE SCAN card and a BLANK, ALIGN, & FOCUS card. These three cards contain 90% of the controls which are peculiar to a given detector head and only the input card bias control will need readjustment when the detector head is changed.

The schematics for these cards appear in Section XII. They are:

(1) HV Card Schematic 111534
(2) Line Scan Card Schematic 111537
(3) Blank, Align, and Focus Card Schematic 111535

5.9 DIGITAL MAGNETIC TAPE CONTROLLER, OPTION -06

5.9A DESCRIPTION

(1) GENERAL. The 1205A-06 Magnetic Tape Controller interfaces the O.M.A. to 8-bit parallel, byte-serial, asynchronous storage media, usually IBM compatible tape recorders such as the Kennedy 1708 or Kennedy 9000 series. The 06 allows recording of compressed data (8 bits/channel), real-time data, or data from memory. An AUTOCYCLE function is provided to automatically record results from repeated experiments.

(2) REAL TIME DATA may be recorded, without loss of data, provided the recorder and buffer/formatter are capable of accepting 15,700 bytes/second (8 bits/byte). If the recording rate is less than 15.7 kilobytes/second, but sufficient buffering to accept 500 bytes/frame is provided, it will be possible to record real-time data, but some frames will have to be lost as the recorder empties the buffer. Real time data are compressed into 8-bit format by converting the digitized output of each channel into 10-bit binary and discarding the two least significant bits. Consequently, the binary number at the output of the 06 option is equal to 1/4 (O.M.A. REAL TIME MAGNITUDE + 100). The offset allows the representation of small negative magnitudes in binary format without the need for a sign bit. The two discarded bits are available on the 06 card should the user want them for a special application.

(3) DATA FROM MEMORY are provided in a three byte per channel format.

BIT #	BYTE 3N		BYTE 3N +1		BYTE 3N + 2	
	0 1 2 3	4 5 6 7	0 1 2 3	4 5 6 7	0 1 2 3	4 5 6 7
	A B R S	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1
	Source & Sign	10^4 digit	10^3 digit	10^2 digit	10^1 digit	Units digit

A = memory A identifier, 1 = data from A memory
B = memory B identifier, 1 = data from B memory
R = reserved bit, hard wired = 1
S = Sign bit, 0 = positive
N = channel number (0 - 499)
The digits are presented in BCD format.

(4) RECORD GAPS AND FILE GAPS. The magnetic tape controller automatically generates an end of record command (EORC) at the end of each frame of real-time data. The tape buffer/formatter translates the End-of-Record command into a record gap. In the data-from-memory mode, channels 0 through 200 constitute one record and an EORC is generated after channel 200. Channels 201 through 499 constitute a second record and, following channel 499, either an EORC or an end of file (EOFC) will be generated. The Kennedy tape buffer/formatter will automatically insert a record gap ahead of the file gap in response to the EOFC so that no EORC is required when the EOFC is given.

The END OF FILE command (EOFC) is given by the tape controller at the end of a measurement sequence, except when this function is disabled by the NO F.C. switch on the 1205A rear panel. Thus if a single frame of data were recorded onto the tape, a file gap would follow it, if a series of frames from either real time (PLOT/PRINT in) or from memory using the autocycle function were recorded, a file gap would be generated following the series of frames. The EOFC may be deleted by placing the F.C. - NO F.C. switch (rear panel of 1205A) in the NO F.C. position.

(5) AUTOCYCLE. The autocycle function is useful when data from memory are to be recorded in a repetitive experiment. The autocycle function initiates a memory erase, accumulation cycle after each set of data is recorded. The number of accumulations may be determined by the O.M.A. preset or full-scale hold functions. The autocycle function may also be used to automatically record the results of manually controlled accumulations or to perform single cycle operation of the O.M.A.

5.9B SPECIFICATIONS

(1) OUTPUT FORMAT, REAL TIME

(a) One byte per channel, 8 bits per byte, straight binary representation of .25 (channel magnitude + 100).

(b) Write Data Strobe, 2 μsec pulse, positive or negative.

(2) OUTPUT FORMAT, DATA FROM MEMORY

(a) Three bytes per channel, 8 bits per byte.

(b) Two blocks, channels 0-200 in block 1; channels 201-409 in block 2.

(c) Source Identifier and Sign, 5 BCD digits per channel.

(d) Three Write Data Strobe pulses, 2 μsec each.

(3) OUTPUT LEVELS AND TERMINATING

(a) TTL Outputs, up to 15 standard loads.

(b) Use twisted pair (120 Ω) impedance, properly terminated for all signal & strobe lines, or use

P.A.R.C. cable assembly (6020-0399-02) to connect to Kennedy tape formatter.

(c) Output polarities may be either positive or negative, factory set, but all data and control lines must have the same polarity. Unless otherwise specified, tape controllers are supplied with proper polarity for Kennedy tape drives.

(4) INPUT CONTROL LINES

(a) Write Ready - indicates tape transport and buffer on line and ready to write data. If false will prevent data dump.

(b) Busy - indicates tape formatter/buffer busy (buffer filled, tape rewriting, etc.) and stops data transfer at end of current record.

(5) DATA INPUT

(a) Real Time - train of pulses proportional to light intensity (1205A COUNT CLOCK D1).

(b) Data from Memory - data are taken in bit parallel, digit serial form from O.M.A. arithmetic card (C4B1).

(6) REMOTE CONTROL

The magnetic tape controller may be controlled remotely by controlling the REALSWDØ, AMEMERSWDØ, BMEMERSWDØ lines which are available via the 1205A TTL REMOTE PROGRAM connector; the AUTOSWDØ line, which is available at the AUTO CYCLE BNC connector; and the ASWDØ, BSWDØ, DIFFSWDØ, and P/PSWDØ which are available at the TTL DIGITAL OUTPUT connector.

(7) RECORDING TIME

A 2400 ft. reel of IBM compatible tape will run approximately 400 seconds in real time.

5.9C REQUIRED ADDITIONAL EQUIPMENT

(1) BUFFER/FORMATTER

The 06 magnetic tape controller is designed to interface with a buffer/formatter with two 1024 byte buffers, and which will generate record and file gaps on command. The Kennedy 9232, 8230, or 1708 with internal formatter/buffer are recommended. For real-time data recording in IBM compatible tape without loss of frames, a minimum tape speed of 37.5 inches per second is required.

(2) CABLE

For use with Kennedy tape recorders, P.A.R.C. cable assembly (6020-0399-02) is recommended.

5.9D OPERATING INSTRUCTIONS

(1) These operating instructions refer specifically to use of the 1205A-06 with Kennedy tape recorders. Use with other recorders will be generally similar.

(2) The tape recorder must be set up according to the manufacturer's instructions. A tape must be mounted on the recorder, with a write enable ring on the feed reel. The WRITE ENABLE light of the recorder should be on, and the recorder should be "on line".

(3) Recording of REAL-TIME data. With O.M.A. in REAL TIME, push PLOT/PRINT to commence recording of real time data. Real time data will be recorded until the PLOT/PRINT switch is released. A frame in progress at the time of release will be completed, and an end-of-record or end-of-file (as selected by F.C. - NO F.C. switch) will be generated automatically. High speed drives (37.5 ips) will keep up to the O.M.A. at any DELAY setting, the 1708 will skip some input cycles at DELAY = 0 or 1, but will keep up at DELAY's of 2 or more. If the recorder has a read-after-write feature, then some input cycles may be skipped if the recorder backspaces to rewrite a block.

(4) DATA FROM MEMORY Mode. When the O.M.A.'s DISPLAY SELECT switches are set for a memory display ("A", "B", or "A–B"), the data from the selected memory mode may be recorded on the tape by pressing the PLOT/PRINT switch momentarily. When the PLOT/PRINT switch is released, the data will be recorded on tape. If the "F.C. - NO F.C." switch on the O.M.A. rear panel is set to the "F.C." position, a file gap will be written at the end of the two-block record. Tape may be conserved by setting the switch to the "NO F.C." position.

(5) The AUTO CYCLE mode performs two functions:

(a) If a measurement ends while the AUTO CYCLE switch is pressed, the data from the selected memory mode will be automatically dumped onto tape as in the DATA FROM MEMORY mode described previously.

(b) If either the A ACCUM or B ACCUM switch is set when the AUTO CYCLE switch is first pressed, or when an AUTO CYCLE memory dump is completed, the corresponding "A" or "B" memory will be erased. The O.M.A. must be in a DISPLAY SELECT mode other than REAL TIME, and the tape transport must be on line with a tape loaded with a write enable ring. If necessary, the AUTO CYCLE mode will wait until these conditions are met before dumping the memory data. When the AUTO CYCLE switch is released, the current measurement/data dump cycle will be completed, but the results will not be erased from the O.M.A. memories, and a file gap will be written on the tape if the "F.C. - NO F.C." switch is in the "F.C." position.

(6) In the MANUAL MEASUREMENT mode, the AUTO CYCLE switch is pressed while both ACCUM switches

are released and not in the REAL TIME mode. If a measurement is made manually by erasing a memory and then accumulating input light by pressing the A ACCUM or B ACCUM switch, releasing the ACCUM switch will end the measurement and cause an automatic recording of the data from the selected memory. The DISPLAY SELECT must be set for the desired memory or memory difference output.

(7) AUTO CYCLE CONTROL. The entire measurement process may be controlled by the AUTO CYCLE function as follows: With the AUTO CYCLE switch released, select the desired memory display mode and input control mode. Set the appropriate A ACCUM or B ACCUM switch and allow the O.M.A. to stop in the PRESET HOLD or FULL SCALE HOLD condition.

When the AUTO CYCLE switch is first pressed, it will erase the memory selected for accumulation, and commence a series of measurement/data-dump cycles. The AUTO CYCLE switch may be operated asynchronously, and the O.M.A. will perform a set of complete measurement/data-dump operations, ending on the completion of the data dump of the measurement that was in progress as the switch was released. Note that, although the AUTO CYCLE switch is operated asynchronously, the actual measurement will start at the beginning of the next complete O.M.A. frame scan.

(8) SINGLE CYCLE. When the O.M.A. is set up as in the preceding section, a momentary operation of the AUTO CYCLE switch will produce at least one complete measurement/data-dump cycle. This control may also be activated electrically via the rear-panel AUTO CYCLE BNC connector. A TTL "low" (sink 1.6 mA to ground) on this connector has the same effect as pressing the front-panel switch. If the line is low for 100 ns or more, an AUTO CYCLE function will take place. This input should be controlled by an "open collector" gate (7403, 7406, etc.), as it is grounded when the front-panel switch is pressed.

(9) BACKGROUND SUBTRACTION. Note that the AUTO CYCLE mode only erases the memory associated with an active ACCUM control. Thus a background measurement may be recorded in the "B" memory, followed by setting A ACCUM and DISPLAY SELECT "A–B". When the AUTO CYCLE button is set, the background stored in the "B" memory will be subtracted from each new "A" memory accumulation before the data is dumped onto the tape.

5.9E AUTO-CYCLE LIMITATIONS

The following conditions should be observed for proper AUTO CYCLE operation:

(1) If the AUTO CYCLE button is set while the O.M.A. is in the REAL TIME mode, switching from REAL TIME to DISPLAY SELECT "A", "B", or "A–B" will be interpreted as an end-of-measurement, and will cause a nonsense record to be dumped onto the tape. The O.M.A. must not be in the REAL TIME mode when the AUTO CYCLE button is set.

(2) If the AUTO CYCLE button has been inadvertently pressed while the tape is off line, or without a write-enable ring, or before the desired measurement setup has been completed, a record may be dumped onto tape when the tape first comes on line, or at the beginning of a measurement. To avoid this, reset as follows:

(a) Release O.M.A. A ACCUM, B ACCUM, AUTO CYCLE, and PLOT/PRINT, and take the tape "off line".

(b) Press REAL TIME.

(c) Press Display SELECT "A".

(d) Press REAL TIME again.

(e) Press desired DISPLAY SELECT pushbutton ("A", "B", or "A–B").

(f) Set tape to "on line".

(3) When doing repeated PRESET HOLD, AUTO CYCLE measurements, the normal dead time between measurements is 32.8 ms. However, the tape controller will hold up for the next measurements as long as necessary to allow a complete data transfer from each measurement. Thus, if the PRESET switch setting is less than 7 with the 1708 tape transport or 2 with the 37.5 ips tape transport, the dead time after some measurement cycles will be increased by one or more 32.8 ms frame times to allow the tape transport to catch up with the O.M.A. data rate.

(4) If the tape transport has the read-after-write option, the time required for a correction rewrite, if longer than the PRESET measurement, will increase the intermeasurement dead time. Increasing the PRESET setting beyond the minimums just mentioned will provide a "cushion" against this eventuality, but, of course, for any PRESET setting there is a length of bad tape which will extend the rewrite process enough to cause an increase in intermeasurement dead time. The best protection against this problem is to avoid the use of poor quality or worn tape.

(5) The internal ANSUB (S2) switch on the O.M.A. TIMING card must be set to the right-hand or NORM position.

5.10 SEQUENCE PRINTER ACCESSORY AND 07 AUTO MODE

5.10A DESCRIPTION

The O.M.A. Sequence Printer is an accessory that allows the PLOT/PRINT output mode to print a subset of the full 500 channels of available output information. This subset is in

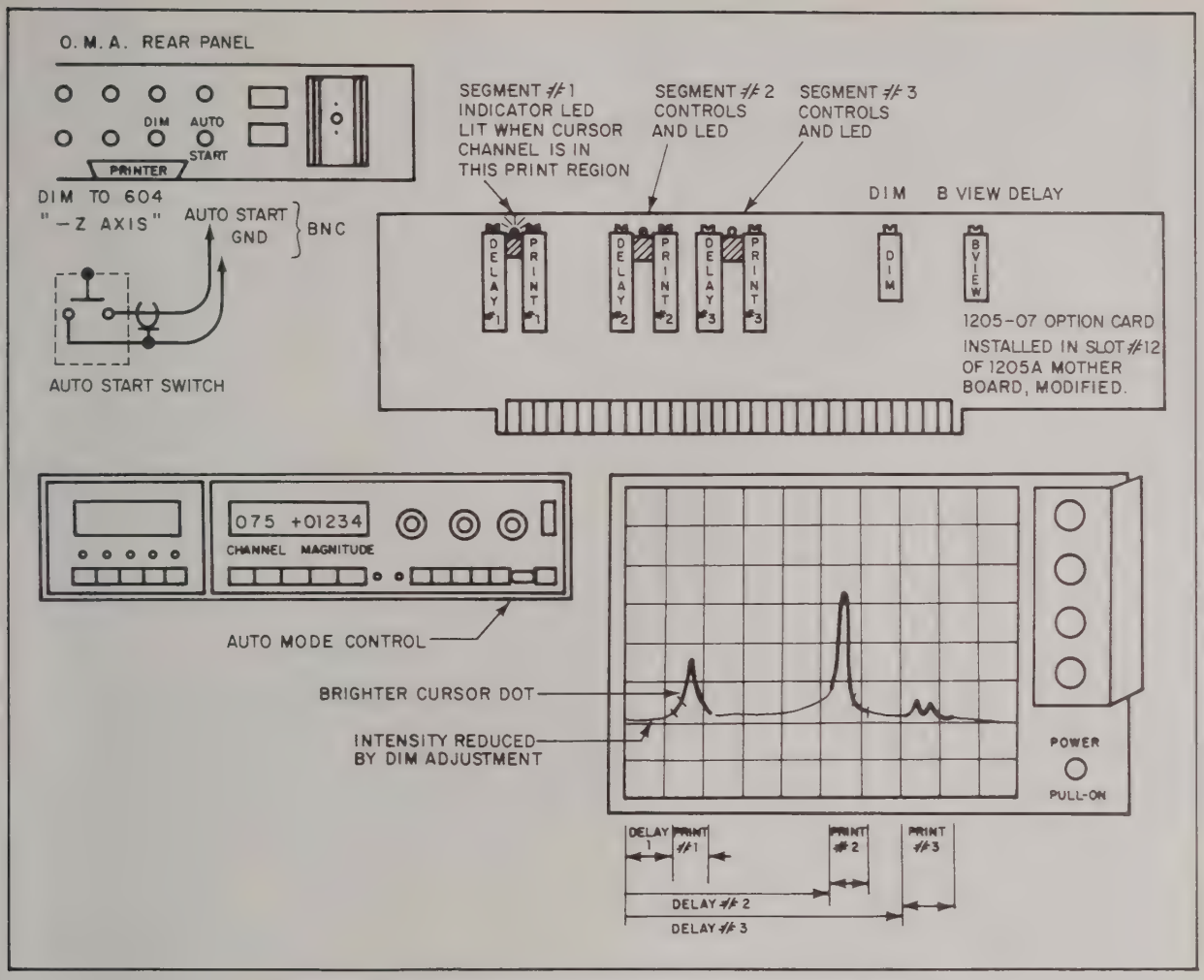


Figure V-5. SEQUENCE PRINTER ACCESSORY AND 07 AUTO MODE

the form of 3 segments of the 500-channel display. Each of these segments can be set from 5 to more than 50 contiguous channels located anywhere within the 500 channels of the standard O.M.A. output.

The segments selected for printout are indicated by brighter sections of the CRT display and by indicators on the option card which glow when the cursor is in one of the selected regions.

07 Auto Mode

The 07 Auto Mode control consists of an extra front panel switch identified as AUTO MODE, and two spare BNC connectors on the O.M.A. rear panel, one labeled AUTO START for the actuating switch and one labeled DIM, which provides the extra display function for the Tektronix 604 CRT display.

When the AUTO MODE switch is released, the O.M.A. will operate as a standard 1205A. When the AUTO MODE switch is pressed, the 07 automatic measurement mode will be activated by pressing a switch or by any other control function that connects the center lead of the AUTO START BNC connector to ground momentarily. Such a switch activation will initiate the following sequence.

(1) While the switch is depressed, the O.M.A. will be in the A MEMORY ERASE and "A" DISPLAY SELECT modes. This allows the CRT display to be used to observe the satisfactory completion of the A memory erasure.

(2) When the switch is released, the O.M.A. will be in the "A–B" DISPLAY SELECT mode as is set on the O.M.A. front panel. The O.M.A. will remain in this condition for a short delay, allowing the user to confirm the continued presence of a prestored background in the B memory by observing the inverted display on the CRT.

(3) After the short delay noted above, an "A" memory accumulation will begin. This accumulation will be terminated by a PRESET HOLD which has been set up on the INPUT CONTROL section of the O.M.A. front panel.

(4) At the end of the preset accumulation process, the O.M.A. will automatically begin the printing output mode. The automatic sequence option will result in the printing of just those channels which are identified by the brighter regions on the CRT display screen. The printing process may be observed by the motion of the intensified cursor dot through these three regions.

(5) On completion of the printing process the O.M.A. will remain in a hold mode displaying the end results of the measurement process. Should there be some apparent difficulty with the measurement as the measurement proceeds, the entire process may be re-initiated at any time during the cycle by pressing the AUTO START control button again.

The AUTO START button is to be provided by the user and connected to the O.M.A. with a standard BNC connector.

5.10B OPERATION OF THE AUTOMATIC MODE ACCESSORY

Preliminary Step

Once the O.M.A. has been set up for the desired print sequence (see adjustment procedure) the following sequence of operations should be performed as a preliminary step to load an appropriate background.

(1) Turn on the system power to the 1205A O.M.A., to the 5055A digital recorder, and to the 604 display scope.

(2) Press the PRESET HOLD and DISPLAY SELECT pushbuttons. Release all remaining pushbuttons.

(3) Set the input control DELAY and PRESET thumbwheel switches for the desired measurement interval.

(4) Press MEMORY ERASE A momentarily. Press MEMORY ERASE B momentarily.

(5) Set up the light input for the normal background or stray light condition.

(6) Press the B ACCUM pushbutton and wait for the accumulation process to end (indicated by the B ACCUM light going out and the PRESET light glowing). Observe appropriate accumulated background on the CRT display.

(7) Press DISPLAY SELECT "A–B".

(8) Press CURSOR ZERO (◂0–) momentarily.

(9) Press the AUTO MODE pushbutton.

(10) Switch the digital recorder from STANDBY to OPERATE if necessary.

(11) Check that sufficient paper is loaded in the printer. The loading sequence is as follows.

(a) Press the small lever at the top left side wall of the paper chamber down. Then latch it.

(b) Insert one-half of a standard pack of paper into this chamber.

(c) Feed the paper into the printer by sliding along the top of the paper chamber towards the rear until the paper is observed feeding out the print slot at the top front of the printer.

(d) Release the paper latch lever at the top left of the paper chamber by pressing the lever in towards the wall and raising it.

(12) Do a sample measurement by applying the appropriate signal light input and pressing the AUTO START pushbutton. Check that the automatic sequence is completed as described in the next section. Check that the printout sections are the desired portions of the 500 channel O.M.A. display by viewing the CRT display. If necessary readjust the printout region as described in the adjustment section.

Measurement Operating Sequence

Once the background has been loaded as previously described, the measurement sequence is as follows:

(1) Establish the experimental input light conditions.

(2) Press and hold the AUTO START pushbutton. Observe a correct erasure of the A memory as indicated by a flat baseline at the zero graticle line of the CRT display.

(3) Release the AUTO START pushbutton and observe that the negative going background display appears correctly on the CRT.

(4) Wait for the completion of the accumulation as indicated by the printer starting to print. The printing process may be observed on the CRT display by watching the cursor dot advance through the 3 print regions and return to zero.

(5) When the process is complete, the printout may be advanced by use of the PAPER ADVANCE control on the printer panel.

Should the printer fail to complete the printing process, check the LOAD PAPER indicator on the printer front panel. Load more paper if necessary. If the output operation is interrupted in this fashion, it may be necessary to re-initiate the instrument by performing one measurement operation to return the print process to the zero position.

From time to time it may be desirable to check the correctness of the prestored background. This may be done by setting up the background input light conditions and pressing the AUTO START pushbutton for a measurement as above. The resulting output should be approximately zero (plus or minus the usual allowance for noise fluctua-

tions) for all 500 channels. If this is not the case, it may be necessary to load a new background measurement as discussed in the previous section.

5.10C CIRCUIT DESCRIPTION 1205-07 SEQUENCE PRINTER WITH AUTO MEASUREMENT CONTROL

General

The following circuit description refers to the IBM print sequence controller, schematic 9083-D-SD (Section XII).

The circuitry on this card provides the necessary control functions to implement the short sequence printing option and measurement control as described in the 1205-07 specification. Some modification of the O.M.A. mother board is required to connect the signal inputs and outputs indicated on this schematic to the corresponding signal points on the O.M.A. mother board.

Automatic Print Sequence

The automatic print sequence is controlled by the three pairs of one-shots, IC's 120 and 102, 122 and 104, and 123 and 107. These six one-shots are arranged in three identical pairs.

IC's 120 and 102 are the controls for the first segment of the automatic print sequence. IC's 122 and 104 are the logic for the second segment of the print sequence, and IC's 123 and 107 control the third segment of the print sequence. Each of these pairs of one-shots provides an identical function. For convenience we will discuss IC's 120 and 102, which control the first print segment.

IC 120 is a NE555 V timer wired to perform the one-shot function. When it is triggered by a high-to-low transition on pin 2, a high level TTL output pulse will appear at the $\overline{Q}$ output pin 3. The duration of this pulse is adjusted by the time constant of R101 and C101. This time constant may be adjusted by the 20-turn trimmer R101. The range of adjustment allowed is from 3.3 ms to approximately 35 ms.

This one-shot, like the corresponding one-shots IC's 122 and 123, is triggered by the frame-retrace interval. The signal FRRETRACEDØ goes low for 384 μs at the beginning of each 32.768 ms O.M.A. frame time. The high-to-low transition of this pulse, buffered by the 2 gates in IC125, triggers the one-shot IC120.

The second one-shot, IC120, is a 74121, a standard 7400 series logic element. This one-shot is triggered by the high-to-low transition which occurs at the end of the time interval of the first one-shot, IC120. The timing components R102 and C102 are selected so that this one-shot may be adjusted from about 0.3 ms and to more than 5 ms, or from about 5 channel times to well over 50 channel times.

Since the one-shot IC120 is triggered at the beginning of each O.M.A. frame time, and generates an output less than one frame time in duration, the second one-shot IC102 will be active or high for a specific portion of each O.M.A. frame cycle. The location within the cycle and duration of this interval are both adjustable. Thus this interval can be used to select any contiguous group of from 5 to 50 or more channels within the 500-channel frame cycle.

In a similar fashion IC122 and 104 select a second interval within the frame cycle, and IC123 and 107 select a third interval within the frame cycle.

The $\overline{Q}$ outputs of IC's 102, 104, and 107 are applied to NAND gate IC109, pins 2, 4, and 5. If any one of the one-shots is active, the corresponding $\overline{Q}$ line will go low, causing the input of gate 9 to be false and causing IC109 pin 6 to go high. This signal is inverted by IC126 (pins 13 and 12) and, via the open-collector buffer IC127 (pins 3 and 4), activates the DIM output. Because of the inversion, this output will have a positive voltage whenever none of the three print-selecting one-shots is active.

A portion of this voltage, adjustable by the DIM trimmer R107, is supplied at the rear panel DIM BNC connector, and is used for the positive-blanking input of the Tektronix 604 scope. This causes the display to be less bright in those regions which will not be printed.

At the same time the output of the NAND gate IC109 pin 6 is applied to the "D" input of flip-flop IC110. This flip-flop is clocked by the buffered ENORD1 signal. This signal appears in the form of five closely-spaced 300 ns high-going clock pulses occurring approximately 3 μs after the beginning of the channel mark time (CHMARKD1). This is the 64 μs interval associated with the channel that has been selected for digital display.

Since the "D" input of flip-flop IC110 will only be high during the 3 intervals set by the one-shots, the flip-flop can only set if the channel selected for digital output is one of the channels which appear in these three one-shot-selected intervals.

If this flip-flop does not set its $\overline{Q}$ output, pin 6 will be high, which enables the second 4-input NAND gate of IC109. If the O.M.A. is in the PLOT/PRINT mode, the signal SLOMODED1 will be high and, if the AUTO MODE has been selected at the front panel, the signal QUICK-PRINTDØ will be low and, via inverter IC126 (pins 1 and 2), will activate IC109 pin 10. Thus, if the channel selected for digital output is not in one of the selected groups of channels, the reset condition of flip-flop IC10 will allow the ENORD1 clock pulses to activate the line number advance clock LNADVCLDKØ to move the channel selector to the next higher-numbered channel.

The timing of the ENORD1 signal is such that the first of the five pulses will cause this line number advance to take place, which in turn prevents the remaining four of the ENORD1 pulses from appearing, and thus prevents the digital output of the previously-selected channel.

After about 60 μs the 64 μs interval for the next-numbered channel will begin, and at that time the preceding sequence will occur again. Thus, during a printing cycle, the selected channel number is advanced as fast as the O.M.A. cycle advances until the channel selected for digital output by the

CHMARKD1 pulse is one of the channels identified by the one-shots of the sequence printer.

When the channel selected for digital output is within one of these selected groups, flip-flop IC110 will set, which will prevent further LNADVCLKDØ pulses from advancing the channel number. Now the channel number advance will be controlled by the normal PLOT/PRINT operation.

If the rear-panel PLOT RATE switch is set for zero, this advance is controlled by the interactive process of the printer's print-command print-inhibit sequence. If the rear panel PLOT RATE control is set for some setting other than zero the channel number will be advanced once every N times 32.768 ms, where N is the number on the rear-panel switch.

As the channel number advances in this fashion, it eventually will arrive at the last of the channels included within a particular one-shot selected channel group, at which point it will again be rapidly advanced by the process previously described to the beginning of the next selected group of channels.

The two inverters, IC126 (pins 11 and 10) and IC126 (pins 3 and 4), and the NAND gate IC125 (pins 11, 12, and 13) are used to control a partial print sequence for use when it is desired to plot the full 500 channels while only printing a selected subset of those channels.

In this mode the SHORTPRINTDØ line is held low by a control switch while the QUICKPRINTDØ line at pin 43 remains high. Thus the rapid advance clocks previously discussed are disabled except when flip-flop IC110 is reset. The print commands are inhibited via NAND gate IC125 (pin 13). Although the PLOT/PRINT sequence proceeds at the normal rate, only those channels that are within the three selected groups will cause the printer to be activated.

In the 07 automatic mode control version, both SHORTPRINTDØ and QUICKPRINTDØ are activated by the front-panel AUTO MODE switch. Thus the instrument is either in the quick short-print mode or in the normal mode.

Note that each of the one-shot $\overline{Q}$ outputs is applied to one of the inputs of the 4-bit storage register, IC108. The load gate (IC108 pin 1) for this register is also activated by the ENORD1 pulses. The three outputs of the storage elements of this register are used to activate light-emitting diode (LED) indication. If the channel selected for digital output is one of the channels selected for printing by one of the three one-shots, the $\overline{Q}$ output of that one-shot will be low as the ENORD1 pulses come high. The storage element for that one-shot will be set in the low condition and the corresponding LED will remain lit for one 32.8 frame time. Thus if the channel selected by the cursor is in one of the printing intervals, the corresponding indicator LED will glow. These LED's will be used to adjust the one-shots by positioning the cursor on a channel and then adjusting the one-shots to cause that channel to be in or out of the selected print interval as desired.

07 Measurement Controller

The 07 measurement sequence is controlled by the circuitry shown at the bottom left of the schematic. If the AUTO MODE switch on the O.M.A. front panel is pressed, the signal AUTOSWDØ will be low and inverter IC130 pin 12 will be high, enabling the operation of this circuit.

The user will provide an AUTO START switch, a momentary contact switch that, when pressed, will connect the signal line AUTOSTARTDØ to ground.

When this line is grounded, inverter IC130 pin 10 will be high, allowing AND gate IC129 through inverter IC130 pin 8 to go low. This will set the erase flip-flop IC128 at pin 4. It will also activate the DISPLAY SELECT A line (ASWDØ), via open-collector buffer IC127 pins 13 and 12. In addition, the erase flip-flop $\overline{Q}$ output pin 6 will activate the MEMORY ERASE A line AMEMERSWDØ via open-collector buffer IC127 pins 11 and 10. Thus, while the switch is pressed, the O.M.A. will be in the DISPLAY MEMORY A and MEMORY ERASE modes.

While this is taking place, the O.M.A. front panel is set for DISPLAY SELECT "A–B", but the internal structure of the O.M.A. is such that activating the ASWDØ line in this mode will cause the O.M.A. output mode to shift to display select A.

When the AUTO START switch is pressed, these lines will also be released. However, flip-flop IC128 will prevent the release of the A MEMORY ERASE line until at least one leading edge of the O.M.A. frame retrace interval occurs. This leading edge provides the low-to-high transition of FRRETD1, which will clock the flip-flop into the reset stage.

This same leading edge will clock the O.M.A. into the memory-erase state since the memory-erase switch line will be active until at least one flip-flop propagation delay after the beginning of the frame blank. Thus, there will always be a memory erasure no matter how short the time interval during which the switch is depressed.

The one-shot IC112 and the first flip-flop of IC131 are a debouncing circuit designed to prevent multiple operations that might occur if the duration of the contact bounce of the auto start switch is long. This circuit functions as follows: The one-shot IC112 is activated by a high-to-low transition on its clock input pin 2. This transition will occur when the AUTO START switch is pressed, allowing the signal line AUTOSTARTDØ to go from high-to-low.

Once a clocking transition activates the one-shot, it will be insensitive to further clocking pulses until the completion of its preset timing interval. This interval is adjusted to approximately 700 ms. The output of the one-shot, a high pulse of fixed duration, is inverted by IC130 pins 5 and 6 and thus the trailing edge of that pulse will provide the low-to-high transition required to clock the first flip-flop of IC131.

If the one-shot has been triggered by contact bounce as the switch is pressed, the "D" input of flip-flop 131 will be low

at the time the clocking transition occurs and thus the flip-flop will not set.

When the AUTO START switch is released, the one-shot will be triggered and, because of its delay, flip-flop 131 will not be clocked until well after the end of any contact bounce in the switch. Since the switch has been released, the D input of flip-flop 131 will be high and the flip-flop will set.

If the switch is pressed for a very short interval, and has sufficient contact bounce to activate the one-shot as the switch is first pressed, the fact that the switch has been released before the one-shot times out will still allow the flip-flop to set.

When the first flip-flop of IC131 sets, it causes a high level to appear on the "D" input of the second flip-flop of IC131. However, this second flip-flop is clocked by the trailing edge of the pulse produced by one-shot IC113. This one-shot is triggered by the high-to-low transition of the $\overline{Q}$ output of the first flip-flop of IC131. Thus the second flip-flop of IC131 cannot set until after the delay of IC113. This delay is adjusted by the B VIEW trimmer.

During this delay interval, the O.M.A. will no longer be in the DISPLAY SELECT A or MEMORY ERASE modes, but will not yet be in the A ACCUM mode. Thus the CRT will display the A–B output selected at the O.M.A. front panel. This allows the background stored in the B memory to be observed in inverted form on the CRT.

At the end of the B VIEW delay, the second flip-flop of IC131 will be clocked into the set condition by the inverted one-shot output via IC130 (pins 3 and 4) and IC129 (pins 1 and 3). When this flip-flop enters the set condition, its $\overline{Q}$ output will go low, activating the A ACCUMULATE switch line AACCUMSWDØ via the open-collector buffer IC127 (pins 9 and 8). At the beginning of the next frame blank interval, the O.M.A. signal accumulation process will begin.

The set condition of the second flip-flop of IC131 will appear on the "D" input of flip-flop 128, preparing this flip-flop to be clocked into the set condition.

At the same time, the low level on the $\overline{Q}$ output pin 6 of IC131 will activate the reset input (pin 13) of the first flip-flop of IC131 via AND gate IC129 (pins 9 and 8). This resets the first flip-flop and places a low signal on the "D" input of the second flip-flop which will be reset by the same transition that will set the flip-flop of IC128.

The signal DELINHD1 is high when no signal accumulation is taking place in the O.M.A., and is low during the signal accumulation process. This line will go low when the accumulation begins after the AACCUMSWDØ is activated, and will go high again when the measurement is terminated. When the measurement is terminated by the PRESET HOLD mode on the O.M.A. input control panel, the low-to-high transition of DELINHD1 will clock the second flip-flops of IC's 131 and 128. This will reset flip-flop 131, effectively releasing the A ACCUM switch line AACCUMSWDØ.

It will also clock the flip-flop 128 into the set condition, allowing the $\overline{Q}$ output of this flip-flop to activate the PLOT/PRINT switch control line P/PSWDØ via the open-collector buffer IC127 (pins 5 and 6). Activating the P/PSWDØ line will cause the O.M.A. to enter the automatic printing sequence controlled by the sequence printer portion of this option card. This printing sequence terminates automatically when the scanning of the 500 channels passes channel 499 and returns to zero.

The O.M.A. will remain in this condition until the AUTO START switch is again pressed to start a new measurement. Pressing the AUTO START switch will cause a low level in AND gate IC129 (pins 12, 11, 4, and 6), which will set the second flip-flop of IC28, ending the PLOT/PRINT mode control function.

At the same time, the signal line resets both flip-flops of IC131 to insure the proper initial conditions for the measurement sequence.

When the AUTO MODE switch on the O.M.A. front panel is released, the signal AUTOSWDØ will be high, resulting in a low level on inverter IC130 pin 12, which also activates the reset line via AND gate IC129 pin 13 and 11. Both flip-flops of IC 131 and both flip-flops of IC128 are therefore forced into the reset condition, preventing any of the signal lines being activated by the auto mode. In addition, the A DISPLAY SELECT switch line ASWDØ is disabled via NAND gate IC130 pin 11. Thus when the AUTO MODE switch is released, the instrument functions as a normal or unmodified O.M.A.

A modified console differs from an unmodified console as follows.

(1) The panel overlay has been cut to open a switch slot between LOG and PLOT/PRINT.

(2) A pushbutton switch has been added in the SPARE MOTHER BOARD location.

(3) Wiring changes as indicated in Table V-4 have been made.

5.11 TWO DIMENSIONAL CARD, OPTION 08

5.11A DESCRIPTION

The 2D Option Card for the 1205A O.M.A. console allows intensity information in two dimensions (X-Y) to be read from the 1205B or 1205D. Data is read by scanning sequential tracks, each of which corresponds to a normal frame scan except with a reduced line scan amplitude. The line scan amplitude is reduced in proportion to the total number of tracks to be scanned. After each track scan (32.8 ms), the dc current in the line scan coil is changed to continually advance the position of successive tracks. The time required for a complete 2D readout will be the product of the number of tracks and the normal frame scan time (32.8 ms).

Data may be accumulated into the 1205A memories from any selected track. This allows signal averaging A–B

baseline correction, and digital readout from any channel in the selected track. The selected track is indicated by intensity modulation on the CRT display and may be positioned by means of a pushbutton slewing control on the 1205A front panel. This control operates in a manner similar to that of the normal cursor controls, except that slewing can be in only one direction.

The number of tracks to be scanned will normally be selected by means of two hexadecimal switches mounted along the top of the 2D Option Card. These switches also control the line scan amplitude to maintain a constant percentage of overlap or underlap between the areas of successive tracks. This percentage is adjustable by means of a trimpot. The hexadecimal switches provide any number

FROM SLOT #12 (Next to Last Slot)	TO	SIGNAL NAME
Pin 20	Slot 11 Pin 20	ENORD1
Pin 21	DIG OUT pin 23 (hole)	LNADVCLKDØ
Pin 22	REM PGM Pin 28 (hole)	FRBLANKD1
Pin 23	REM PGM Pin 3 (hole S10P15	FRRETRACEDØ
Pin 24	N.C.	PRINTCMD2DØ
Pin 25	N.C.	PRINTCMDØ
Pin 26	Shielded wire to SPARE BNC "DIM"	DIMA+
Pin 27	SPARE BNC "AUTO START"	AUTOSTARTDØ
Pin 29	Slot 8 Pin 29	SLOMODED1
Pin 31	DIG OUT Pin 46 (hole)	P/PSWDØ
Pin 32	REM PGM Pin 50 (hole)	AACCUMSWDØ
Pin 33	DIG OUT Pin 14 (holes w/jumper)	ASWDØ
Pin 34	REM PGM Pin 48 (hole)	AMEMERSWDØ
Pin 36	REM PGM Pin 29 (hole)	DELINHD1
Pin 41	SPARE Mother Board SWITCH, rear contacts	AUTOSWDØ
Pin 42	Slot 12 Pin 41	SHORTPRINTEDØ
Pin 43	Slot 12 Pin 42	QUICKPRINTDØ
	SPARE Mother Board SWITCH, center contacts to ground	

Two spare rear-panel BNC connectors labeled DIM and AUTO START are added.

A front-panel pushbutton switch is added and labeled AUTO MODE.

Table V-4. MODIFICATION WIRING FOR 07 OPTION

of tracks from 1 to 256. The number of tracks and the selected track may also be remotely controlled through a 25 pin connector installed on the back panel of the 1205A. A switch is provided on the back panel to change from normal (1D) operation to 2D operation.

All computer interface and data recording techniques used for normal O.M.A. operation may also be used with the 2D Option Card. These include option cards for teletypewriter interface and for 9-track digital tape recorders. Using a real-time computer interface, signal averaging and data collection can be optimized for a large number of tracks or for selected portions of selected tracks. The output data rate using the 2D option card is the same as for conventional O.M.A. operation (15.6 kHz or 64 μs per sample), and is independent of the number of tracks. An analog output signal is available for real-time tape recording or external A/D conversion.

Two types of CRT Y and CRT Z display are provided, one of which presents intensity information as small Y axis displacements with a normal CRT Z input. The second display type uses a CRT Z input taken from the 1205A CRT Y output line so as to present a 2D picture, similar to a conventional TV picture. These display modes are controlled with trimpot adjustments on the 2D Option Card.

5.11B CIRCUITS

The 2D Option Card for the 1205A O.M.A. allows the use of the 1205B/D/F detector heads in a two-dimensional rather than a one-dimensional mode. The 2D operation is achieved by modifying the current waveform in the line scan coil. The modified current consists of two superimposed waveforms, one of which is a reduced version of the triangular waveform produced by the O.M.A. line scan card. The second waveform is a stepped ramp which steps after each 32.8 ms frame scan. By this means a number of mini-frames or tracks are produced at successively displaced regions on the target of the tube.

The two binary counters U25 and U26, with outputs fed through D/A converter U27, generate the stepped ramp referred to above. At the end of the ramp, with all counter outputs high, flip-flop U23 changes state and allows *one* of the FRRETD1 pulses to be converted into the STROBE1DØ pulse which loads the counters U25 and U26. The counters are preset to numbers generated by the hexadecimal switches S5 and S6. Thus, the total number of steps is given by $N_1 + 16N_2$, where N_1 is the number read on S5, and N_2 is the number on S6. The number of tracks is one more than the number of steps (not counting the retrace steps).

With the hexadecimal switches set to zero, the number of tracks can be remotely controlled by selectively grounding the inputs to counters U25 and U26. With the REMOTEDØ line low, the counters are preset after each frame time so that the number of tracks can be arbitrarily changed from one frame time to the next.

The current output from D/A U27 is converted to a voltage by operational amplifier U30A. The buffered line scan waveform from operational amplifier U30B is also added into the summing junction of operational amplifier U30A. The D/A converter U29 in the feedback path of operational amplifier U30A provides a gain which is inversely proportional to the number of tracks, thus keeping the total scanned area independent of the number of steps in the ramp. The line scan signal at the output of operational amplifier U30A varies with the number of tracks to keep a constant percentage of underlap between successive track areas. This percentage is adjusted with trimpot R14. Trimpot R16 controls the dc voltage at the output of operational amplifier U30A and thus controls the vertical position of the scanned area.

U32 is an impedance converter with unity voltage gain, and its output drives the 1205B/D/F line-scan coil. Trimpot R17 controls the input voltage to U32 and thus controls the height of the scanned area on the tube.

The dual operational amplifier U34 generates a voltage for driving the vertical axis of a CRT which displays the 2D information. One half of U34, acting as a differential voltage amplifier, separates the stepping ramp voltage from the 15 kHz line-scan waveform. The stepping ramp waveform is added to a portion of the CRT Y output waveform in the second half of U34. Trimpot R23 adjusts the amplitude of the CRT Y output signal which is fed through the 2D CRT Y output, thus providing a series of vertically displaced conventional O.M.A. type traces. For a picture type display with a large number of tracks, R23 would be set fully counterclockwise so that no ΔY would be produced from the CRT Y signal.

The remaining circuitry provides for the selection of one track for accumulation into memory, signal averaging, baseline subtraction, and CRT display. Counters U7 and U8 store an 8 bit number representing the selected track, and the digital comparators U9 and U10 provide an output at the time the selected track is scanned by the electron beam in the detector.

The selected track may be changed by use of the front-panel track select switch. Depressing this switch allows inverted FRRETD1 pulses to advance the count in counters U7 and U8. To allow for the advance of just one track at a time, counter U2 provides a 10-frame delay between the first and second pulses applied to counter U7. If the track select switch is released before the second pulse, the track select counter is incremented only once. This operation is identical to that of the cursor control pushbuttons on the 1205A front panel.

The selection of a track for accumulation or display may be computer controlled in either of two ways. Since comparators U9 and U10 have dual inputs, the second set of inputs can be interfaced to a computer output. The computer selected track comparator output pulse appears at pin 11 of U21 if the REMTRKSELDØ line is lowered. If this line remains high, the gating circuitry of U21 causes the selected track to remain under control of counters U7 and U8.

The second method of computer (or external digital) control for track selection is to apply an appropriate pulse

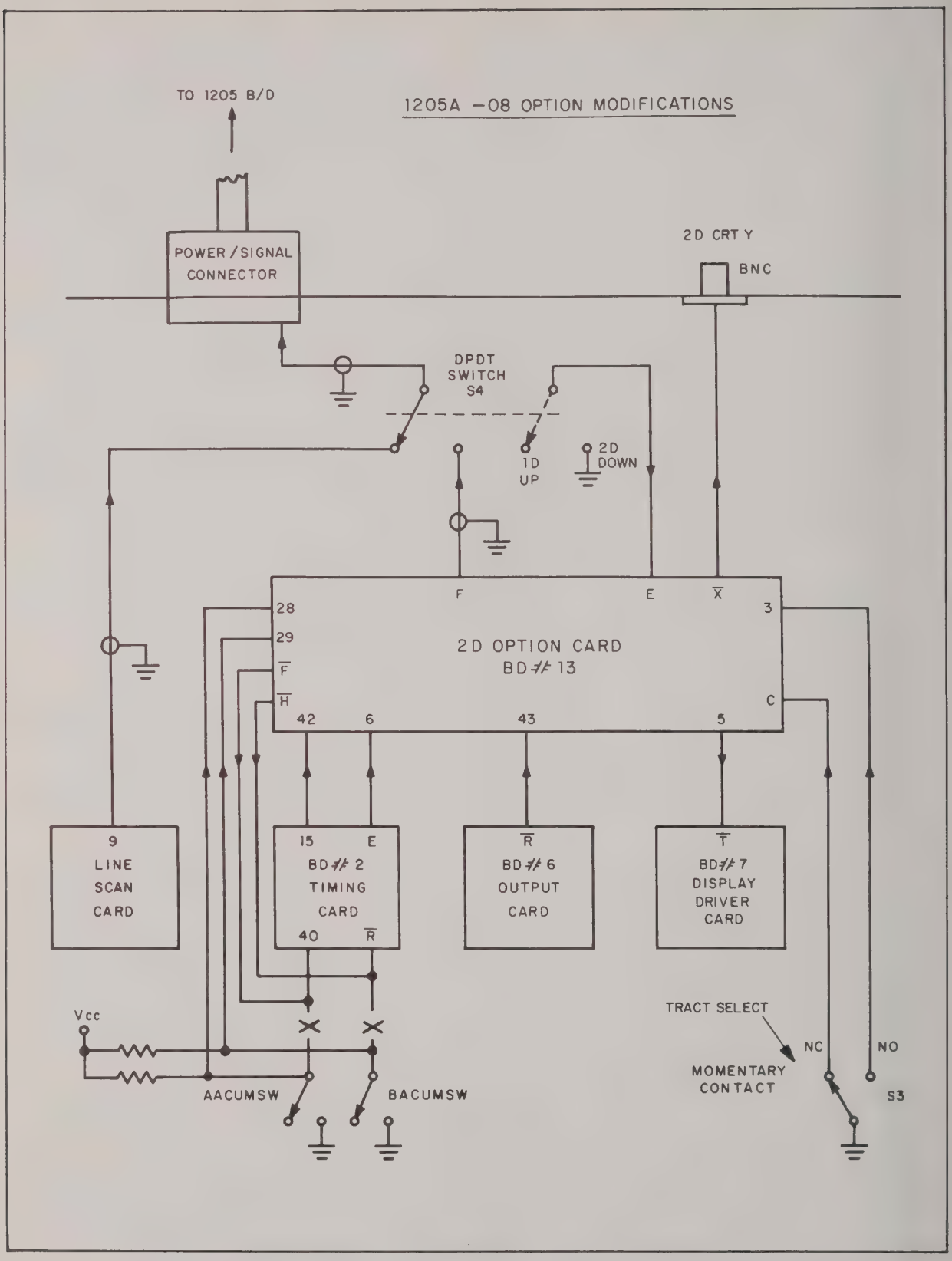


Figure V-6. TWO-DIMENSIONAL OPTION BLOCK DIAGRAM

train in parallel with the control line from the front-panel Track Select switch. Although this second method reduces the number of digital control lines required for interfacing, it may require more external interface circuitry to generate the pulses.

If the track select comparator inputs are not within the range of the outputs from counters U25 and U26 for any given number of tracks, there will be no comparator output. In this case, the circuit composed of U20 and half of U1 will cause a strobe pulse to be applied to counters U7 and U8. The strobe pulse loads these counters with the number appearing on the inputs of counters U25 and U26. In this way the selected track as controlled from the front panel will be initialized to the proper range independent of the total number of tracks.

With the 2DMODEDØ line low, the NOR gates of U22 prevent accumulation into memory A except during the time of the selected track. With switch S4 in the normal position, memory B is also inhibited except during the selected track scan. However, with S4 in the dual spectrum position, memory B will accumulate during all tracks except the selected track. In this way, using two tracks, one track will accumulate into the A memory and the other track will accumulate into the B memory (dual spectrum operation). With the 2DMODEDØ line high the NOR gates of U22 act as two pairs of series inverters so that normal 1D mode accumulation into the memories is achieved. However, with S4 in the dual spectrum position, simultaneous accumulation into both A and B memories is not possible.

Because of gate and comparator delays, the 2D mode accumulation into memory is delayed by one frame time from the comparator output pulse. The D type flip-flop U23 is used to compensate for this delay and to provide a CRT Z axis pulse to indicate the location of the selected track. Trimpot R5 adjusts the amplitude of this Z-axis pulse.

5.11C OPERATION AND SETUP

To use the 2D Card with an appropriately modified 1205A console, the following steps are required:

(1) Insert the card in the rearmost socket with the components facing forward (slot 13).

(2) Connect a Tektronix Model 605 storage display to the 1205A as shown in Figure V-7.

Note that the 2D CRT Y output BNC is directly below the CRT Z high connector.

(3) On the display driver card, place the CRT Z high polarity switch in the left hand (negative position.

(4) If proper 1D operation of the system has been verified, place the mode control toggle switch on the back panel in the 2D position (down).

(5) On the timing card, place the background subtract switch in the OFF (left hand) position.

(6) On the input card, adjust the bias trimpot to place the dark current baseline in the region of zero counts per frame per channel.

(7) On the 2D Option Card, set the desired number of tracks using the hexadecimal switches. The number of tracks is $1 + N_1 + 16N_2$, where N_1 is the number on the left-hand switch and N_2 is the number on the right-hand switch.

(8) If accumulation from a single track is desired, set the SPDT slide switch (S5) on the 2D card to the "normal" (left hand) position. If accumulation in the dual spectrum mode is desired, set the switch to the "dual spectrum" (right hand) position. The dual spectrum mode provides alternating accumulation into

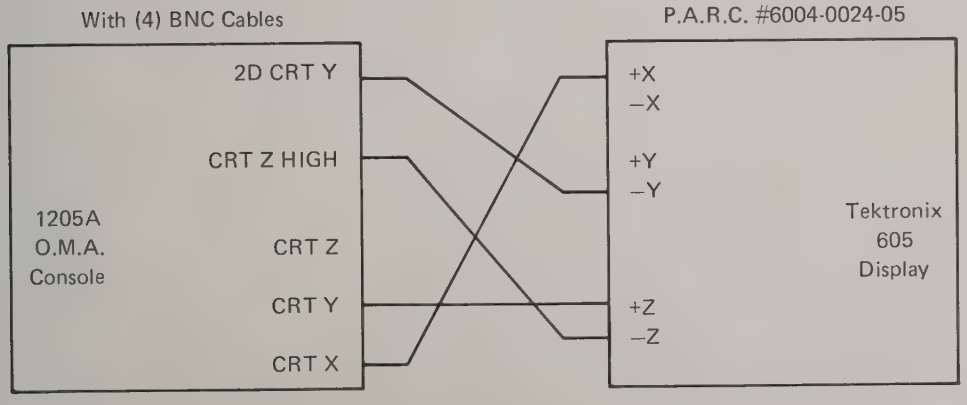


Figure V-7. 2D INTERCONNECTIONS WITH SCOPE

the A and B memories from the selected track and from all other tracks respectively. This mode is generally used with just two tracks. Both A and B accumulate buttons must be pressed to accumulate in the dual spectrum mode.

If the trimpots on the 2D Option Card have been properly adjusted, a 2D raster pattern should now be present on the 605 display. An intensified horizontal track will appear at the bottom of the display, and an intensified vertical line (or set of spots) will appear at the cursor channel location. The intensified track may be slewed vertically by depressing the front-panel track select pushbutton. Data will be accumulated into the memories only from the selected track.

On the 2D Option Card, the trimpot functions from left to right are:

(1) Selected Track Intensity, R5 (Display Monitor)

The selected track-intensity trimpot controls the differential intensity on the selected track through the CRT Z and CRT Z HIGH outputs. With a fully CCW setting, the selected track will *not* be intensified.

(2) 2D CRTΔY, R23 (Display Monitor Y Amplitude)

The display 2D CRTΔY trimpot controls the signal level at the 2D CRT Output connector. With this control fully counterclockwise, there will be no coupling to this connector, and each track on the 2D display will appear as a straight line. In the fully counterclockwise position, there is no Y signal, and Z modulation from the CRT Y connector is used to provide the picture. Clockwise rotation increases the Y signal amplitude, providing a 1-D type display for each track.

(3) 2D Track Height, R14 (Detection Scan Control)

The 2D track-height trimpot adjusts the line-scan amplitude as a percentage of the spacing between tracks. This percentage may be greater or less than 100%. With a low (counterclockwise) setting, the signal readout will be low and a baseline oscillation will appear. This oscillation results from moire interference between the raster pattern and the diode array pattern. As the track width is increased (clockwise rotation), the moire oscillation will decrease and the desired signals will increase. With no signal present, the dark current baseline will increase. Normally, the track height is adjusted to be equal to or greater than the track separation, with up to 50% overlap. In making these adjustments, it is helpful to have a real-time video display using a non-storage CRT connected to the CRT X, CRT Y, and CRT Z outputs. This display is also useful for maximizing the dynamic range using the cathode and bias trimpots.

(4) 2D Vertical Position, R16 (Detector Pattern Position)

The vertical position trimpot is used to center the 2D raster pattern on the camera tube axis. This will also result in a dc component in the line-scan coil current.

(5) 2D Vertical Size, R17 (Detector Pattern Size)

The vertical size trimpot controls the distance between the first and last track, both on the camera tube and on the 2D display through the 2D CRT Y output. With a maximum setting (fully clockwise), the scanned dimension on the camera tube is approximately 0.5 inches.

Using RCA silicon target tubes at room temperature, dynamic range and resolution are satisfactory with up to 64 tracks. Operation up to the maximum number of tracks will be possible with certain other types of tubes or with moderate cooling of the silicon target tubes.

Optimization of performance at high track numbers requires careful adjustment of the track width, target voltage, bias, and beam current (G1) controls. Generally, at track numbers greater than 64, the dynamic range will be limited by target saturation and dark current (even with optimum adjustments), rather than by the 1205A A to D Converter.

5.12 1200 SERIES CABLES FOR ACCESSORIES

The necessary cables required to operate the 1205 Optical Multichannel Analyzer Instruments with the appropriate accessories are listed in Table V-5. Cable drawings are provided in Section XII with the schematics.

Cable Model No.	Instrument/Accessory used with		Purpose/Function	Cable Length	Cable Schematic
	From	To			
C0328	1205A	1205B, D, E, & G	Power/Signal cable, O.M.A. console to Detector	6 ft	110328
C0398	1205A	1205KB, KD, KE, & KG	Power/Signal cable, O.M.A. console to Detector	6 ft	110398
C0320	1205D	1210 or 340	MHV High Voltage cable for gating 1205D with 1210 or 340 Pulser	6 ft	110320
SC0024	1205A	604	BNC Signal cable, O.M.A. console to 604 Monitor	3 ft	110322
C0375	1205A	5055A (unmodified)	Interface (Data/Command) cable, O.M.A. console to 5055A Digital Printer (without H49 codewheels)	6 ft	110375
C0380	1205A	5055A-H49	Interface (Data/Command) cable, O.M.A. console to Standard 5055A-H49 Digital Printer	6 ft	110380
C0383	1205A	4070	Interface (Data/Command) cable, O.M.A. console to 4070 Facit Tape Punch; character-serial; bit parallel	6 ft	110383
C0382	1205A	33TBE-ASR Teletype	Interface (Data/Command) cable, O.M.A. console to 33TBE-ASR Teletype	15 ft	110382
C0390	1205A	1207	Power/Signal cable, O.M.A. console to 1207 Extended Delay Accessory	4 ft	110390

Table V-5. 1200 SERIES CABLES FOR ACCESSORIES

SECTION VI
CALIBRATION

6.1 GENERAL

This section covers the adjustment of the input card and the various analog display outputs (i.e., the large cards plugged into the main mother board at the right of the O.M.A. console). These adjustments must be performed with the Detector Assembly disconnected. Adjustment of the Detector Assembly drive electronics (small cards - see Section VIII) requires a correctly set up CRT display as described here and in Section VII.

The calibration procedure in this section is based on the standard output settings and the use of a standard CRT display as described in Table VI-1 (e.g., standard factory adjustment and Tektronix 604 scope). However, these procedures may also be used to adjust the O.M.A. to accommodate any reasonably similar CRT display. This means any display with 70 to 160 millivolts per division X- and Y-axis inputs, and a sensitive dc Z-axis input requiring less than 5 volts to go from full blank to full intensity.

OUTPUTS (Standard Setting)

CRT display Standard: 8 x 10 divisions, 100 mV/div. 0 V blank +1 V = full intensity.

CRT X (BNC) 0 to +1 V x-axis drive ramp

CRT Y (BNC) -.5 V to +.5 V Full Scale

CRT Z (BNC) -.2 V blank, +.4 V nominal brightness level, +0.9 V Cursor Dot

Plotter Standard: 100 mV/division
10 x 15 divisions (PLOT RATE = 9)
10 x 10 divisions (PLOT RATE = 6)

PLOT X (BNC) 10 mV/second ramp, 0 to 1.5 V (max with INT-ADJ = 2.2 V)

PLOT Y (BNC) -1 V to +1 V Full Scale, 33 to 360 ms/channel
150 s/500 channels, PLOT RATE = 9
100 s/500 channels, PLOTE RATE =6

OUTPUTS (Adjustment Range)

CRT X 0 V to (0 to +1.5) volts (150 max mV/div.)

CRT Y -.8 V to +.8 V Full Scale max.
-.33 V to +.33 V Full Scale min. (70 to 160 mV/div.)

CRT Z Nominal brightness level: -1 V to +1 V
Blank level: 0 to 1 V more negative than nominal brightness level
Cursor dot: 0 to 1 V more positive than nominal brightness level

CRT Z HI Positive or negative-going, any three levels in the range of -10 V to +10V

CURSOR 64 μs TTL pulse, high during cursor-selected channel time.

PLOT X 0 to +65 mV/s ramp, +2.2 V max.

PLOT Y 2 times CRT Y output level, no separate adjustment

VIDEO Output similar to REAL TIME mode CRT Y, but usable during A ACCUM.
5.0 V = approx. 500 counts, output range adjustable from 0 to 1 V/100 counts

Table VI-1. STANDARD CRT DISPLAY

Triggered scopes with no X-axis input and scopes with a high level Z-axis input or no Z-axis input are covered in Section VII - USE OF NON-STANDARD SCOPES.

The Calibration Table, Table VI-2 at the end of this section, comprises a summary of the standard adjustment steps, testpoints and calibration levels.

6.2 SMALL CARDS WARNING

The trimmers on the small card installed on the System Power board at the left of the O.M.A. console determine the electronic focus and alignment of the Detector Assembly. DO NOT CHANGE THE SETTING OF ANY OF THESE CONTROLS. Misadjustment of one of these controls may require that the entire Detector Assembly drive electronics adjustment procedure of Section VIII be performed.

If there is reason to believe that these cards are grossly misadjusted (e.g., if one or more of the small cards has been replaced), refer to Section VIII before connecting the Detector Assembly.

6.3 ADJUSTING THE CRT TO THE O.M.A. CALIBRATION

This procedure covers the adjustment of the CRT display to an already calibrated O.M.A. This adjustment would be performed if the CRT display is changed, or if the O.M.A. is set for particular output levels and it is not desirable to change them.

(1) Set the O.M.A. controls as follows.

DELAY switch: Ø
PRESET switches: Ø999
PRESET HOLD: set
TEST: set
"A" DISPLAY SELECT: set
remaining pushbuttons: released
SCALE FACTOR: 10^3
DISPLAY EXPAND
VERT: CAL
HORIZ: CAL

(2) Set the CRT display range controls (if any) for the appropriate range. This is normally 100 millivolts per division for both axes.

(3) Connect:

O.M.A. Rear Panel	CRT Display
CRT X output: (BNC)	X-axis (horizontal; positive input)
CRT Y output: (BNC)	Y-axis (vertical; positive input)

Do not connect the Z (intensity) axis at this time.

(4) Turn on the O.M.A. and CRT display. Press the O.M.A. MEMORY ERASE A pushbutton momentarily. After the CRT display has had time to warm up, adjust its intensity control for a visible line.

(5) Adjust the CRT display position controls to position this line over the desired "zero" graticule line, with the left edge of the display line at the left edge of the graticule area. For the normal 8 x 10 division display, the "zero" graticule line is the second line up from the bottom edge of the screen.

(6) Adjust the CRT display X-axis (horizontal) gain control so that the display line is exactly the width of the graticule area (10 divisions). Figure VI-1 shows the location of the gain trimmers on the Tektronix 604 accessory CRT display.

(7) Turn the O.M.A.'s HORIZ DISPLAY EXPAND control fully clockwise. If the O.M.A. is not already at CHANNEL ØØØ, press the cursor zero (0) control momentarily.

(8) Set the REAL TIME pushbutton. The CRT display should look like Figure VI-1a if the TEST signal is adjusted for 100 counts. Note that when the O.M.A. power is off, the beam is positioned in the lower lefthand corner of the screen, allowing the operator to select the desired display brightness with the CRT display intensity control.

6.4 PREPARATION FOR 1205A CALIBRATION

Remove the O.M.A. console top cover by removing the two black rack-mounting bracket screws on each side of the Model 1205A console (8-32 high tensile, 3/32" socket head), and the four 8-32 phillips-head screws nearest the edges of the bottom of the console. The top cover is then removed by sliding it to the rear and off the O.M.A. chassis.

Figure VI-2 shows a top view of the uncovered O.M.A. chassis, and identifies the circuit boards, testpoints, and calibration adjustments. Each card is also identified by including the card name in the P.C. artwork. Except for the INTEGRATE card (card 11), the large cards are all labeled at the top righthand corner of the card. The testpoints and controls are also identified by labels on the artwork. For layout reasons, the INTEGRATE card (card 11) is labeled at the top left, and the trimmers on the OUTPUT card (card 6) are identified on the back of the card.

CAUTION

HIGH VOLTAGES are present on the small cards (HV card), the Detector Assembly signal/power connector, the AC power input area at the left rear corner of the console, and other areas.

Use an insulated alignment tool to avoid circuit damage caused by accidental P.C. board shorts.

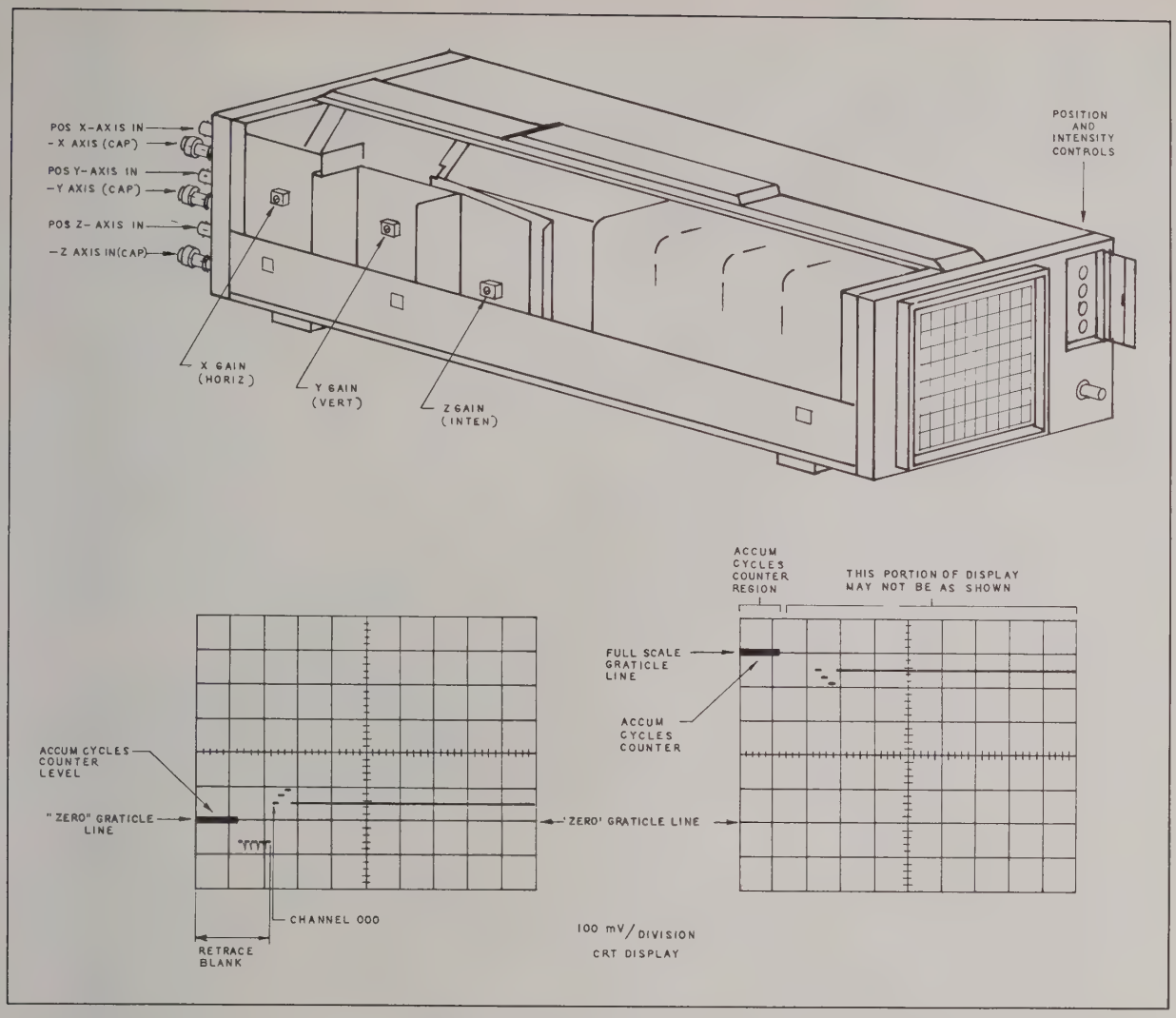


Figure VI-1. MODEL 604 CRT DISPLAY

The initial settings for the O.M.A. controls are as follows.

DELAY switch: Ø
PRESET switches: 1ØØØ
PRESET HOLD: set
TEST: set
"A" DISPLAY SELECT: set
remaining pushbuttons: released
SCALE FACTOR: 10^3
DISPLAY EXPAND
VERT: CAL
HORIZ: CAL

INTERNAL SWITCHES (large cards)

Preset-Delay Reversal (two slide switches at left of the PRESET card, #9): NORM (both set to the right)
CRT Z HIGH polarity (slide switch on DISPLAY DRIVE card, #7): "–" (set to the left)
Analog Subtract (S2 on the TIMING card, #2): NORM (set to the right)
MEMORY OFFSET (S1 on the TIMING card, #2): 100 (set to the right)

The 1205B POWER/SIGNAL (Detector Assembly) Cable should be disconnected.

6.5 POWER SUPPLY

Measure the +5 V supply output at the right end of R6 on the System Power board.

> **CAUTION**
> This testpoint is located just behind the HIGH VOLTAGE card.

Adjust the "+5 V ADJ" trimmer on the System Power board (Figure VI-2) to set this voltage at +5.00 volts, ±0.1 V.

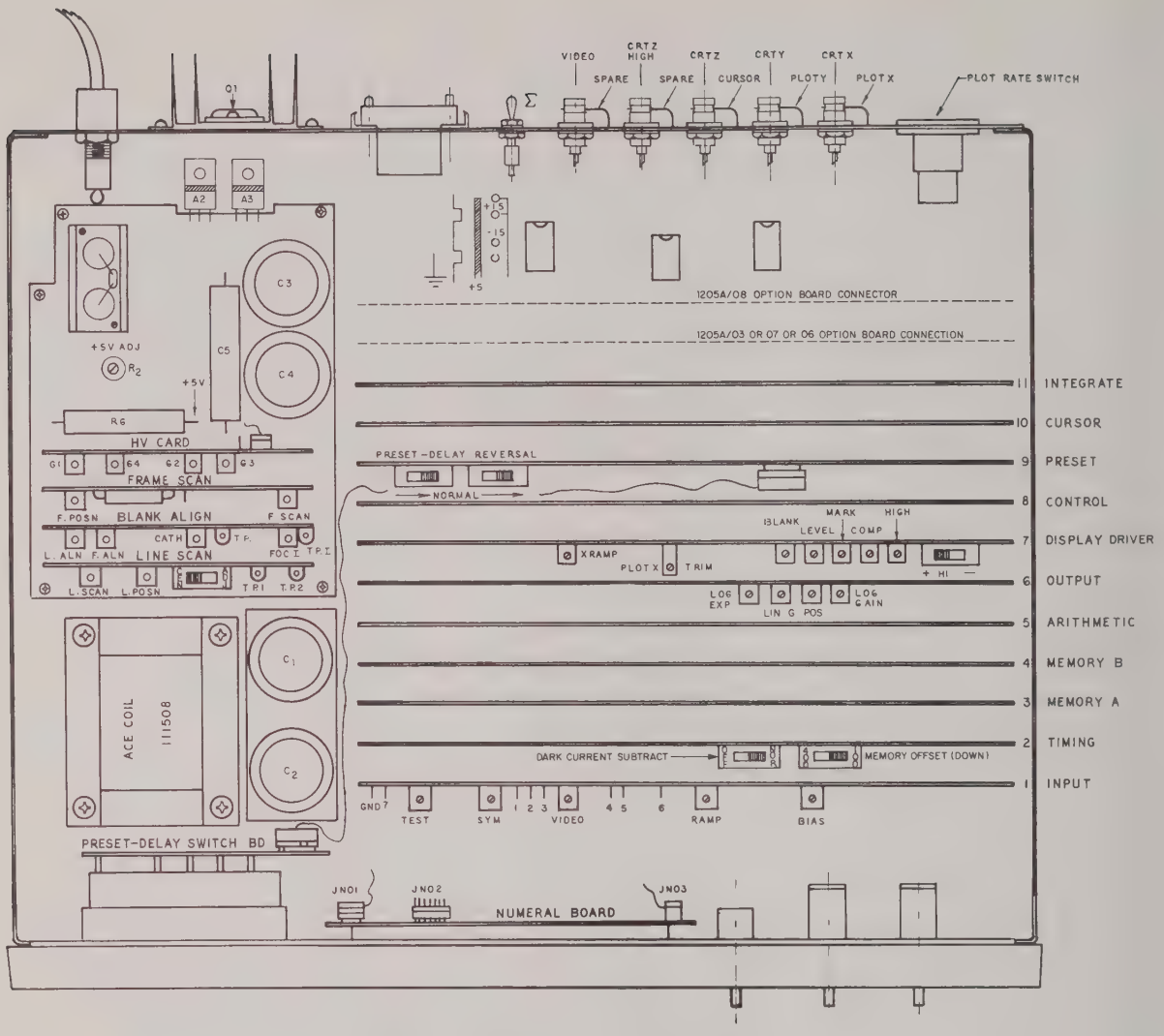


Figure VI-2. TOP VIEW OF O.M.A. INTERIOR

6.6 CRT DISPLAY CALIBRATION

The O.M.A. is adjusted at the factory to drive a Tektronix Model 604 Display. The recommended display sensitivity is 100 mV/div for both axes. Instructions for adjusting and operating the display are provided in the Tektronix Instruction Manual.

6.7 CRT X (SWEEP) ADJUSTMENT

Set the HORIZ DISPLAY EXPAND control to the CAL position.

6.7A STANDARD CRT X

NOTE: If this procedure is used, skip 6.8B.

Using a general-purpose oscilloscope set for .2 V/div sweep, observe the CRT X output of the O.M.A. Adjust the X RAMP trimmer (located to the left of the center of the DISPLAY DRIVER card, #7) for a 1.0 V pk-pk amplitude in the observed sawtooth.

6.7B ADJUSTMENT TO CRT DISPLAY

Connect the positive X-axis (horizontal) input of the CRT display to the O.M.A. CRT X output. Adjust the position and intensity controls of the CRT display to produce a horizontal line on the screen, with the left end of the line at the left edge of the graticule area. Adjust the X RAMP trimmer on the DISPLAY DRIVER card (#7) so that the display line is exactly the width of the graticule area.

If the CRT display has a 10 division, 100 mV/division horizontal input, this results in the standard O.M.A. setting.

6.8 CRT Y (VERTICAL) ADJUSTMENT

6.8A SETUP

The following sequence prepares the O.M.A. for this adjustment.

DELAY switch: Ø

PRESET switches: 1000
PRESET HOLD: set
ACCUM CYCLES: set
"A" DISPLAY SELECT: set
"A" MEMORY ERASE: pressed momentarily

Set A ACCUM and wait for the accumulation to stop automatically at A ACCUM CYCLES MAGNITUDE = 1000, with the PRESET HOLD indicator glowing, and the A ACCUM indicator out. Release the A ACCUM pushbutton.

PRESET switches: 0001
"B" DISPLAY SELECT: set
"B" MEMORY ERASE: pressed momentarily

Set the B ACCUM pushbutton and wait for the accumulation to stop automatically at B ACCUM CYCLES MAGNITUDE = 1, with the PRESET HOLD indicator lit, and the B ACCUM indicator out. Release the B ACCUM pushbutton.

LOG: set
SCALE FACTOR: 10^3
DISPLAY EXPAND, VERT: CAL

6.8B OSCILLOSCOPE (STANDARD ADJUSTMENT)

NOTE: If this procedure is used, skip 6.8C.

To adjust the CRT Y output to the standard setting using a general purpose oscilloscope, set the scope up as follows.

(1) Sweep: 200 μs/division.

(2) Trigger: Connect the oscilloscope external trigger input to the O.M.A. CURSOR output (rear panel BNC). Adjust the scope to trigger on the positive-going edge of the 4 V, 64 μs cursor pulse. (Check triggering by connecting the scope vertical to the cursor output.)

(3) Vertical Input: Connect to the CRT Y output of the O.M.A. Set vertical scale factor at 100 mV/division (if the scope has at least five vertical divisions).

(4) Set the O.M.A. cursor controls for CHANNEL = 499. The region from 120 μsec to 500 μsec from the left of the oscilloscope display is the ACCUM CYCLES counter region referred to in the adjustment procedure, Subsection 6.8D.

6.8C ADJUSTMENT TO CRT DISPLAY

To adjust the CRT Y output to the CRT display (or to the standard setting if the CRT display is a 100 mV/division display), set up as follows.

(1) Connect the CRT display positive X-axis (horizontal) input to the CRT X output of the O.M.A. Adjust per Subsection 6.7B if necessary.

(2) Set the O.M.A. cursor controls for CHANNEL = 000.

(3) Turn the HORIZ DISPLAY EXPAND knob to the fully clockwise position.

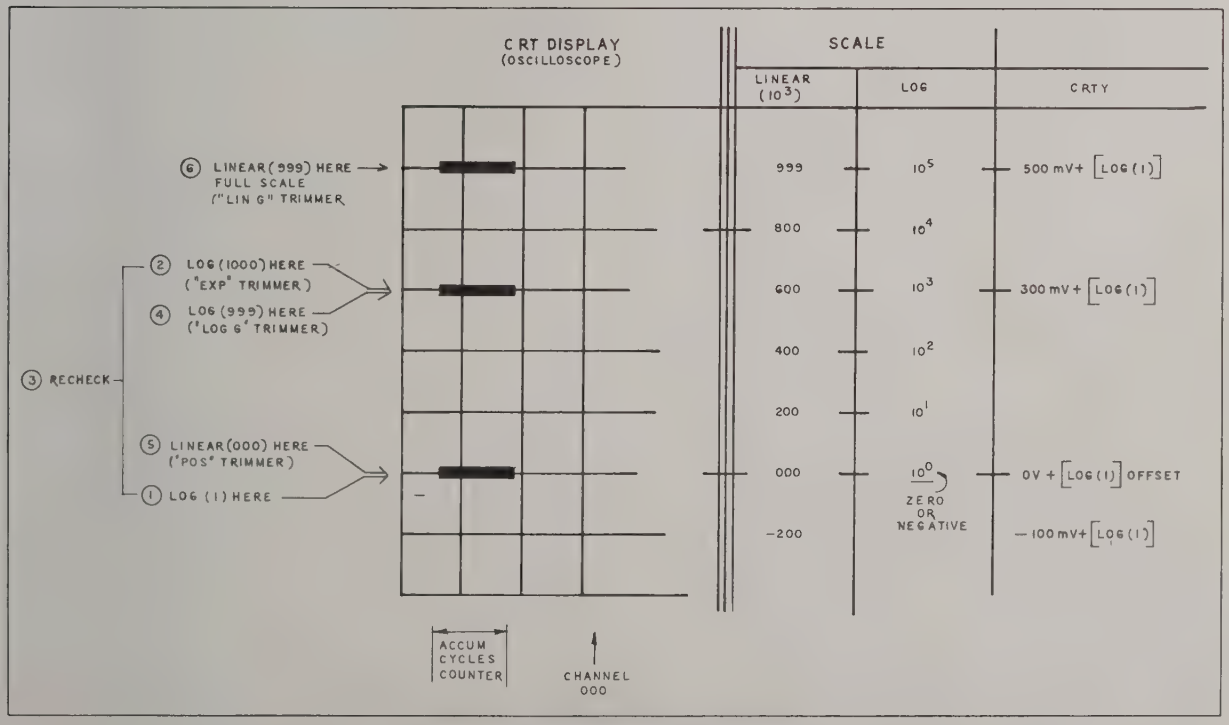


Figure VI-3. OUTPUT CARD - STANDARD CRT Y ADJUSTMENT

(4) Connect the CRT display positive Y-axis (vertical) input to the CRT Y output of the O.M.A. This input scale factor must be in the range from 70 to 160 mV per division.

The region from 1/2 division to two divisions on the expanded CRT display is the ACCUM CYCLES counter region referred to in the adjustment procedure in the next paragraph. This region is part of the retrace blank when the CRT Z intensity control is connected to the display. The CRT display intensity control may be turned up to override the CRT Z signal in this case.

6.8D CRT Y PROCEDURE - STANDARD

The four trim pots on the OUTPUT card (#6) are adjusted to calibrate the Y-axis (analog MAGNITUDE) outputs of the O.M.A. From left to right, they are the *log exponent* (EX), linear gain (LIN G), linear position (POS), and log gain (LOG G) controls. These are labeled on the back of the OUTPUT card.

Once the O.M.A. is set up as described in the previous paragraphs, the ACCUM CYCLES counter portion of the display can be conveniently switched from one calibration level to the next by use of the DISPLAY SELECT controls.

The calibration procedure is as follows (see Figure VI-3).

(1) Select *log (1)*, - (DISPLAY SELECT "B" & "LOG"). The ACCUM CYCLES display region will normally show a small offset - typically less than ±1/2 division (±50 mV). This level is the reference level for all CRT Y adjustments. Adjust the CRT display (oscilloscope) vertical position control to position the ACCUM CYCLES counter region over the "zero" graticule line. For the normal CRT display, this is two divisions up from the bottom of the display area.

(2) Select *log (1000)*, - (DISPLAY SELECT "A" & "LOG"). Adjust the *log exponent* trimmer (left-most OUTPUT card trimmer, "EX") to position the ACCUM CYCLES display region over the 10^3 graticule line. For the normal CRT display, this is three divisions up (+300 mV) from the "zero" [*log (1)*] level in step (1).

(3) The log exponent setting may affect the *log (1)* level slightly. Repeat steps (1) and (2) until both levels are correct.

(4) Select *log (999)*, - (DISPLAY SELECT "A–B" & "LOG"). Adjust the *log gain* trimmer (right-most OUTPUT card trimmer - "LOG–G") to position the ACCUM CYCLES region over the 10^3 graticule line. There should be no noticeable level shift while switching between DISPLAY SELECT "A–B" and "A" [*log (999)* and *log (1000)*].

(5) Select linear zero (release "LOG", select "A"). 1000 appears as zero in the linear, SCALE FACTOR = 10^3, mode. Adjusat the *linear position* trimmer (third from right on OUTPUT card, "POS") to position the ACCUM CYCLES display region over the "zero" graticule line. There should be no level shift between *log (1)* (step 1) and linear zero (step 5).

(6) Select linear 999 (release "LOG", select "A–B"). Adjust the *linear gain* trimmer (second from right on OUTPUT card, "LIN G") to position the ACCUM CYCLES display region over the full-scale graticule line. For the normal CRT display, this is five divisions (+500 mV) up from the "zero" level in steps (1) and (5).

6.8E ADJUSTMENT FOR BALANCED DISPLAY

In most normal and background subtraction applications, the negative signal outputs or "A–B" differences are small. However, some applications may result in large negative signal differences. This is particularly true when the input conditions require the use of the balanced or "400" mode (see Subsection 6.14).

For these applications the CRT Y output may be calibrated for a balanced CRT display presentation which displays the full negative dynamic range of the instrument (to –99999) at the expense of some loss of display resolution in the normal positive signal area. The LOG mode presentation remains as in the standard display, since the LOG output cannot go negative and does not display negative outputs.

The setup and calibration procedure are the same as the standard procedure described in the preceding section (6.8D) except that the format is modified as follows (see Figure VI-4).

(1) In step (5) the linear position trimmer ("POS") is adjusted to position the linear zero over the display center graticule line. For the standard 8 x 10 division, 100 mV/div display, this results in a two division (or +200 mV) positive level shift from *log (1)* (step 1) to linear zero (step 5).

(2) In step (6) the linear gain trimmer (LIN G) is adjusted to set the *linear 999* level at the top edge of the display. For the standard 8 x 10 division, 100 mV/div display, this is four divisions (+400 mV) above the "linear zero" level, or an absolute voltage of +600 mV (six divisions) plus the *log (1)* offset of step (1).

6.9 CRT Z (INTENSITY) ADJUSTMENT

The CRT Z output provides an intensified marker on the CRT display to indicate the channel selected for digital display. It also serves to blank the display during the retrace and interchannel intervals. The output is determined by the BLANK, LEVEL, MARK, and COMPENSATE trimmers located at the right end of the DISPLAY DRIVER (#7). These trimmers are labeled between the controls, and by the letters B, L, M, and C at the top edge of the card.

6.9A STANDARD SETTING

Connect the oscilloscope to the O.M.A. CRT Z output, and set up as follows.

(1) Sweep: 200 μs/div.

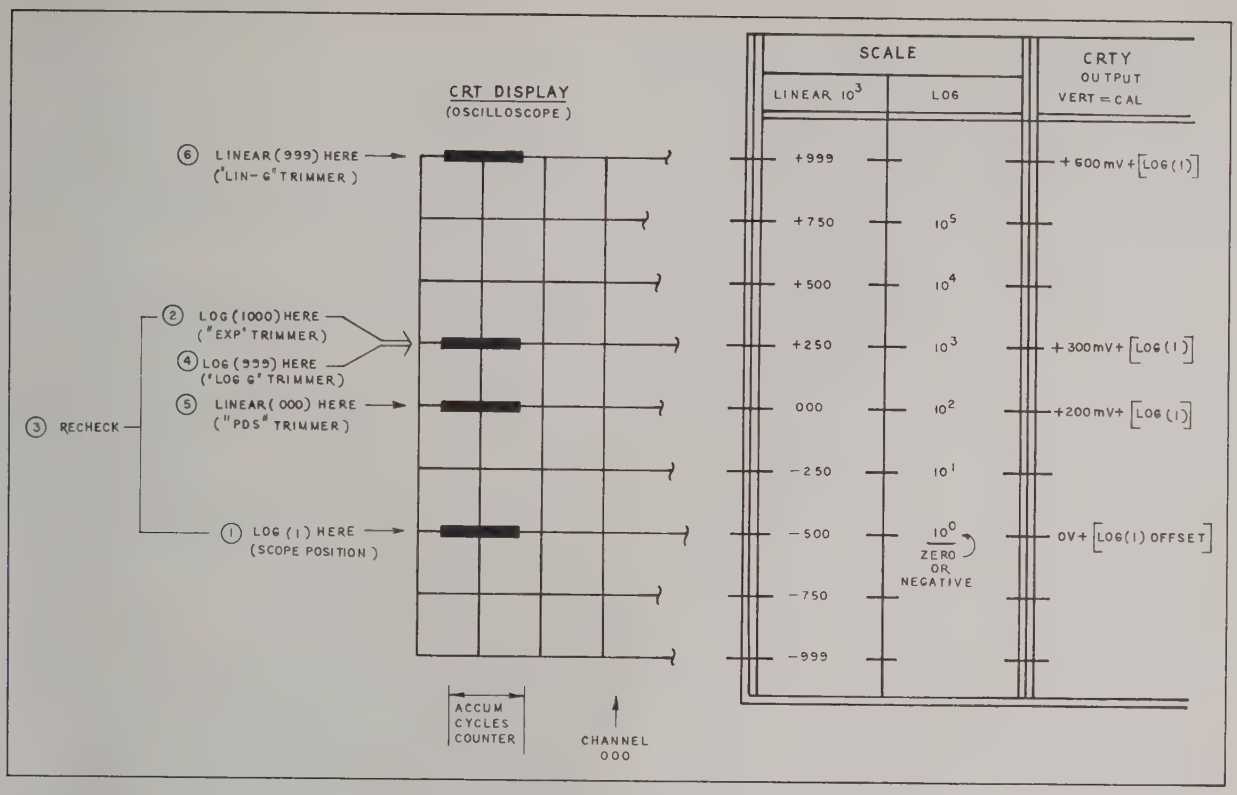


Figure VI-4. OUTPUT CARD - BALANCED DISPLAY CRT Y ADJUSTMENT

(2) Trigger: Connect the oscilloscope external trigger input to the O.M.A. CURSOR output, and adjust to trigger on the positive-going transition of the +4 V, 64 μs cursor pulse.

(3) Vertical Scale: 200 mV/div.

(4) Set the scope zero to view a +1 V to −.2 V signal.

(5) Set the O.M.A. cursor to CHANNEL = 499.

(6) Set the O.M.A.'s HORIZ DISPLAY EXPAND control to the CAL position.

Figures VI-5a and VI-5b show the CRT Z signal after the adjustment has been completed. The procedure is as follows. **NOTE:** If this procedure is followed, skip 6.9B.

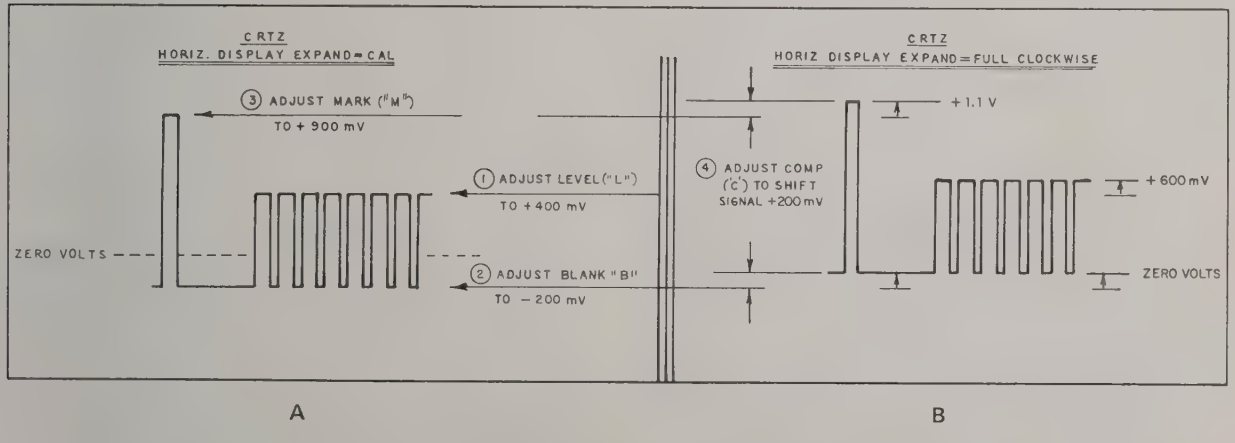


Figure VI-5. CRT Z

(1) Adjust the DISPLAY DRIVER card LEVEL trimmer ("L", fourth from right) for +400 mV basic intensity level.

(2) Adjust the BLANK trimmer ("B", fifth from right) for −200 mV blanking level (the 700 μs low region).

(3) Adjust the MARK trimmer ("M", third from right) for +900 mV cursor level (the first 64 μs on the scope).

(4) Turn the HORIZ DISPLAY EXPAND control fully clockwise. Adjust the COMPENSATE trimmer ("C", second from right) so that the entire CRT Z signal is shifted +200 mV from the CAL level. (Level = +600 mV, Blank = 0 V, Mark = +1.1 V, as shown in Figure VI-5b.)

6.9B ADJUSTING CRT Z TO DISPLAY

This paragraph assumes that the CRT display can be driven from full blank to full intensity by less than +2 V. Adjustment is as follows.

(1) CRT X should be adjusted per Subsection 6.7.

(2) With CRT X, CRT Y, and CRT Z all disconnected, adjust the CRT display intensity control so that the display dot is just barely extinguished.

(3) Connect CRT X to the display horizontal input, and CRT Z to the display's positive intensity input.

(4) Turn the O.M.A.'s HORIZ DISPLAY EXPAND knob to the CAL position.

(5) Adjust LEVEL trimmer ("L") on the DISPLAY DRIVER card (#7) to produce a display baseline just slightly brighter than normal viewing level. If this control is turned fully clockwise (indicated by clicking at the limit of travel) without producing a satisfactory brightness level, refer to Subsection 6.10, CRT Z HIGH.

(6) Position the O.M.A. cursor at CHANNEL = 250.

(7) Turn the MARK trimmer ("M") on the DISPLAY DRIVER card (#7) clockwise to produce an intensified dot on the baseline, at the center of the display (Channel 250). This control should be set at the minimum clockwise adjustment that produces a satisfactory contrast.

(8) It may be necessary to reduce the LEVEL setting ("L" counterclockwise) somewhat to achieve the best compromise between brightness and cursor contrast. This depends on the brightness range of the CRT display.

(9) Position the O.M.A. cursor at CHANNEL - 495.

(10) Set the HORIZ DISPLAY EXPAND control fully clockwise.

(11) Turn the COMPENSATE trimmer ("C") on the DISPLAY DRIVER card (#7) fully counterclockwise, and then turn it clockwise until a satisfactory expanded-mode brightness level is achieved.

(12) Turn the BLANK trimmer ("B") fully counterclockwise, and then turn it clockwise until the 12 channels between 499 and ØØØ are just blanked, and gaps appear between adjacent channels. Turn the BLANK trimmer one-half turn further clockwise.

6.10 CRT Z HIGH

NOTE: Skip this procedure if display is standard Tektronix 604.

The CRT Z HIGH output can accommodate intensity inputs that require more than +2 V, and can be inverted to accommodate negative (blanking) intensity inputs. In general, dc-coupled inputs requiring up to 8 V swing from blank to full intensity can be conveniently handled. High-level, ac-coupled cathode type intensity inputs present additional problems, and are covered in Section VII, Subsections 7.1C and 7.3.

The CRT Z HIGH output consists of a polarity switch and variable-gain amplifier attached to the CRT Z output. The HIGH ("H") trimmer and (−HIGH+) switch are located at the far right end of the DISPLAY DRIVER card (#7).

The adjustment procedure is as follows.

(1) Adjust the CRT Z output to the standard setting as described in Subsection 6.9A.

(2) Turn the CRT Z HIGH trimmer ("H" DISPLAY DRIVER card) counterclockwise until it clicks at the adjustment limit. Then turn the trimmer 5 turns clockwise.

(3) Set the (−HIGH+) switch for the signal polarity that will intensify the CRT display. If this is not known:

  (a) Set HORIZ DISPLAY EXPAND fully clockwise.

  (b) Connect CRT X to display horizontal input.

  (c) Set display intensity control to just blank the display.

  (d) Connect CRT Z HIGH to intensity input.

  (e) Set O.M.A. cursor at CHANNEL = 499.

  (f) When the (−HIGH+) switch is correctly set, there will be a bright line segment at the left of the display, followed by a blank segment of equal width, followed by a bright line extending off the screen to the right.

(4) With all display inputs disconnected, adjust the CRT display intensity control to just blank the beam.

(5) Connect CRT X (adjusted per Subsection 6.7) to the display horizontal input.

(6) Set the O.M.A. HORIZ DISPLAY EXPAND control to the CAL position.

(7) Set the O.M.A. cursor to CHANNEL = 250.

(8) Connect CRT Z HIGH to the display intensity input.

(9) Adjust the CRT Z HIGH trimmer ("H", DISPLAY DRIVER card) to obtain a reasonably satisfactory baseline brightness and cursor dot.

(10) Adjust the LEVEL, MARK, BLANK and COMPENSATE controls, following the procedure in Subsection 6.9B.

6.11 PLOT Y

There is no separate adjustment for the PLOT Y output. When activated, by pressing the PLOT/PRINT control, the PLOT Y output scale factor is twice the CRT Y output scale factor set in Subsection 6.8.

6.12 PLOT X

The PLOT X output provides a slow voltage ramp to provide a sweep drive for plotter output. The ramp rate is set by the 30-turn PLOT RAMP trimmer, located at the bottom of the DISPLAY DRIVER card (#7) between the X RAMP trimmer and the Z-axis trimmers. The label on the PLOT RAMP trimmer cannot be seen when the cards are installed, but the control may be seen by looking down between the OUTPUT card (#6) and the DISPLAY DRIVER card (#7), just to the left of the BLANK ("B") trimmer. *Use only an insulated alignment tool to set the PLOT RAMP trimmer,* to avoid shorting nearby circuitry. There are four approaches to setting the PLOT RAMP control, depending on the application and equipment available.

6.12A PLOT X RATE METHOD

(1) Set the PLOT RATE switch (back panel) to zero.

(2) Connect a voltmeter to the PLOT X output.

(3) Determine the ramp rate required to meet the conditions discussed in Subsection 4.3B(2) for your plotter. The standard setting is 10 mV per second.

(4) Press the PLOT/PRINT control and adjust the PLOT RAMP control to achieve the desired ramping rate. Turning the control clockwise increases the ramping rate.

(5) The PLOT X output will limit at just over +2.2 V. If the PLOT RAMP setting is not complete, release the PLOT/PRINT control momentarily to reset the PLOT X output.

6.12B PLOT X FULL SCALE METHOD

This method is time consuming, but eliminates the requirement for a sensitive voltmeter.

(1) Set the PLOT RATE switch (rear panel) to the desired setting, as discussed in Subsection 4.3B(2), and determine the corresponding plotter full scale input requirement. (Standard setting: PLOT RATE = 8., +1.5 V full scale.)

(2) Set the cursor to CHANNEL = ØØØ by pressing the cursor zero control (⟵0⟶) momentarily.

(3) Press PLOT/PRINT and observe the PLOT X output voltage.

(4) If the PLOT X output voltage exceeds the desired full-scale level, release the PLOT/PRINT switch and turn the PLOT RAMP trimmer counterclockwise.

(5) When the channel number goes from 499 to ØØØ, the channel advance will stop, and the PLOT X output will hold at the full scale (500 channel sweep) output level. If this voltage is too high, turn the PLOT RAMP trimmer counterclockwise. If it is too low, turn the trimmer clockwise. Release the PLOT/PRINT control.

(6) Repeat steps (2) through (5) until the PLOT X output is the correct full-scale level at the end of the 500 channel scan.

6.12C CALIBRATION TO PLOTTER

This section calibrates the O.M.A. to a standard X-axis gain setting of the plotter.

(1) *If the INPUT card (#1) has not been calibrated,* set REAL TIME and TEST. If the MAGNITUDE reading is *not* positive, turn the TEST trimmer on the INPUT card (leftmost trimmer, card #1) clockwise to obtain a positive reading. If turning the TEST trimmer fully clockwise does not result in a positive MAGNITUDE, adjust the card as in Subsection 6.13, Input Card Calibration.

(2) Set up the plotter Y (MAGNITUDE) axis as described in Subsection 4.3B(1). Note that this assumes correct calibration of the CRT Y output (see Subsection 6.8).

(3) Select an appropriate PLOT RATE setting to meet the requirement of the plotter as discussed in Subsection 4.3B(2). Set the PLOT RATE control on the O.M.A. rear panel to this value.

(4) Turn the 15-turn TEST trimmer on the INPUT card (#1) fully counterclockwise. Set the TEST and REAL TIME pushbuttons and *record the MAGNITUDE* reading.

(5) Adjust the BIAS trimmer on the INPUT card (rightmost trimmer, card #1), for a MAGNITUDE reading of exactly +200.

(6) Set the DELAY switch on the O.M.A. front panel to one less that the PLOT RATE setting from step (3) (e.g., PLOT RATE = 9, DELAY = 8).

(7) Set up the O.M.A. as follows.

PRESET switches: 0499
PRESET HOLD: set
TEST: set
"A" DISPLAY SELECT: set
remaining pushbuttons: released
SCALE FACTOR: 10^5
DISPLAY EXPAND
HORIZ: CAL
VERT: CAL
"A" MEMORY: Erased (press MEMORY ERASE A momentarily)
CURSOR: CHANNEL = ØØØ (press ⊸0⊸ momentarily)

(8) Set the plotter X-axis gain to the desired level (normally 100 mV/div), and connect the input to the PLOT X output of the O.M.A.

(9) Draw a straight line on the plotter paper, from the CHANNEL ØØØ, MAGNITUDE = ØØØØØ point to the CHANNEL 499, MAGNITUDE = +99800 point.

(10) Position the plotter pen over the Channel ØØØ, MAGNITUDE = ØØØØØ point, using the plotter's X-position and Y-position controls.

The O.M.A. is now set to accumulate from zero to full scale (+99800) and stop in exactly the same time that the PLOT/PRINT Mode will require to scan through the 500 channels. When the 500-channel PLOT/PRINT operation is complete, the PLOT X ramp output will stop and hold its ending value until the PLOT/PRINT switch is released. When the O.M.A. is correctly adjusted, pressing the A ACCUM and PLOT/PRINT controls simultaneously as in the next step will cause the plotter to duplicate the line drawn on the plotter paper in step (9).

(11) Simultaneously press both the A ACCUM control and the PLOT/PRINT control.

(12) Adjust the PLOT RAMP trimmer (DISPLAY DRIVER card #7, at the bottom of card just left of the Z-axis trimmers) until the plotter pen is moving *parallel* to the line drawn on the paper. It is not necessary that theplotter line coincide with the drawn line.

(13) Release the PLOT/PRINT control if necessary to prevent the pen from limiting.

(14) Re-initialize the O.M.A. as follows.

PLOT/PRINT: released
A ACCUM: released
A MEMORY: erased (press MEMORY ERASE A momentarily)
CURSOR: CHANNEL = ØØØ (press ⊸0⊸ momentarily)

(15) Repeat steps (11) through (14) as necessary to complete the adjustment. When the adjustment is completed, steps (14) and (11) will cause the plotter to duplicate the drawn line. If the plotter position controls are properly set and step (11) is done correctly, the 500 steps of the plotter line will be just below and touching the drawn line.

(16) Set the O.M.A.'s REAL TIME and TEST pushbuttons and reset the BIAS trimmer on the INPUT card (right-most trimmer, card #1) to the MAGNITUDE reading recorded in step (4).

(17) Set the TEST trimmer (left-most trimmer on the INPUT card, #1) to the desired test signal level (usually MAGNITUDE = 100).

6.12D 100 mV/SEC PLOT X

If the O.M.A. has been adjusted to the standard CRT Y output calibration, the following procedure will set the PLOT X output to the 100 mV/second sweep rate. Any sensitive differential voltmeter may be used, but an autopolarity digital voltmeter or differential oscilloscope is preferred as these are less sensitive to input overload.

(1) Turn the 15-turn TEST trimmer on the INPUT card (#1) fully counterclockwise. Set the TEST and REAL TIME pushbuttons and *record the MAGNITUDE reading.*

(2) Adjust the BIAS trimmer on the INPUT card (right-most trimmer, card #1), for a MAGNITUDE reading of exactly +200.

(3) Set up the O.M.A. as follows.

PLOT RATE switch (rear panel): 6
DELAY switch: 5
PRESET switches: 0499
PRESET HOLD: set
TEST: set
"A" DISPLAY SELECT: set
remaining pushbuttons: released
SCALE FACTOR: 10^5
DISPLAY EXPAND
HORIZ: CAL
VERT: CAL
"A" MEMORY: erased (press MEMORY ERASE A momentarily)
CURSOR: CHANNEL = ØØØ (press ⊸0⊸ momentarily)

This step allows the O.M.A. to accumulate to +99800 in the same 3000 frame times that the PLOT/PRINT mode will require to scan through the 500 channels. When both the A ACCUM and PLOT/PRINT pushbuttons are simultaneously set, the PLOT Y output will advance in 2 mV steps from zero to +0.99 V in 98.3 s, while the PLOT X output ramps upward from zero at an adjustable rate. Thus the PLOT Y output provides a reference ramp to calibrate the PLOT X output. Note that this is only true if the CRT Y output is set for the standard 0.5 V full scale calibration.

(4) Connect the differential voltmeter between the PLOT X output (+) and the PLOT Y output (—). Use a range such as ±200 mV f.s. If a conventional mechanical meter is to be used, make a preliminary adjustment of the O.M.A., at a ±1 V range setting to avoid the possibility of "pinning" the meter.

(5) Simultaneously press both the A ACCUM control and the PLOT/PRINT control.

(6) Adjust the PLOT RAMP trimmer (card #7, DISPLAY DRIVER, at the bottom of the card just left of the Z-axis trimmers) until the differential voltage stops changing, indicating that the two outputs are changing at the same rate. If the setup is as in step (4), turning the trimmer clockwise will cause the difference to go more positive or less negative. It is not necessary to bring the difference voltage to zero.

(7) Release the PLOT/PRINT control if necessary to keep the meter from limiting.

(8) Re-initialize the O.M.A. as follows.

PLOT/PRINT: released
A ACCUM: released
"A" MEMORY: erased (press MEMORY ERASE A momentarily)
CURSOR: CHANNEL = ØØØ (press 0 momentarily)

(9) Repeat steps (5) through (8) as necessary to complete the adjustment of the PLOT RAMP trimmer.

When correctly set, the difference voltage between PLOT X and PLOT Y will remain at the initial offset throughout the entire PRINT/PLOT scan. This offset voltage is typically on the order of ±50 mV, plus the effect of not pressing A ACCUM and PLOT/PRINT simultaneously in step (5). The offset due to step (5) error will be corrected at the end of the 500-channel scan as the CHANNEL number advances from 499 to ØØØ and stops. At this point both outputs will be at +0.99 V ±5% relative to ground, and the difference may drift slightly due to residual drift in the PLOT X hold level.

Note that if the calibrating instrument used is a dual-trace scope in the subtract mode, the common-mode input range of the instrument may be exceeded at less than +0.99 V. This may result in spurious effects during the latter portion of the 500-channel scan, which should be ignored.

(10) Set the O.M.A.'s REAL TIME and TEST pushbutton and reset the BIAS trimmer on the INPUT card (right-most trimmer, card #1), to the MAGNITUDE reading recorded in step (1).

(11) Reset the TEST trimmer on the INPUT card (left-most trimmer, card #1) to the desired test signal MAGNITUDE, usually +100.

6.13 INPUT CARD

This section covers the standard or initial setting of the trimmers on the INPUT card (#1). The SYMMETRY, RAMP, and BIAS trimmers calibrate the scan beam chopping and input analog-to-digital conversion circuits, and these adjustments may be modified somewhat to accommodate the characteristics of a specific Detector Assembly. This is covered in Section VIII, Adjustment of Detector Assembly Drive Electronics. In general, the RAMP trimmer controls the A-D conversion factor, and its setting may be modified to calibrate the O.M.A. at a specific wavelength. The BIAS and SYMMETRY controls are adjusted from the nominally correct settings in this section to accommodate non-uniformities in the vidicon target.

The TEST and VIDEO trimmers control the uncalibrated test mode input and analog video output signal levels. They may be set to any convenient level.

6.13A RAMP (A—D CALIBRATE) ADJUSTMENT

Connect an oscilloscope to the ramp testpoint TP-6, located just to the left of the RAMP trimmer on the INPUT card (#1). Adjust the RAMP trimmer for exactly 10.0 V pk-pk at the testpoint. The RAMP is not adjustable on units with serial numbers less than 1000.

6.13B BIAS ADJUSTMENT

The RAMP adjustment must be completed before setting the BIAS trimmer. The BIAS adjustment is as follows.

(1) Set the TEST and REAL TIME pushbuttons. Release all remaining pushbuttons.

(2) Turn the TEST trimmer on the INPUT card fully counterclockwise, until clicking is heard at the control limit.

(3) Adjust the BIAS trimmer on the INPUT card for a zero O.M.A. REAL TIME MAGNITUDE reading (MAGNITUDE = +00000).

6.13C SYMMETRY ADJUSTMENT

The RAMP and BIAS adjustments must be completed before setting the symmetry (SYM) trimmer. *It is imperative that the TEST pushbutton be released and the Detector Assembly disconnected before starting this procedure.*

(1) Set the REAL TIME pushbutton. Release all remaining pushbuttons.

(2) Disconnect the Detector Assembly at the rear panel 1205B POWER/SIGNAL connector.

(3) Check that the TEST pushbutton is *not* depressed.

(4) Connect a small dc voltage in the ±2.0 V* range between TP-1 on the INPUT card and ground. TP-1 is located just to the right of the symmetry (SYM) trimmer on card #1.

*Approximately +4 V is available at the right end of resistor R29, a 470 Ω resistor located at the lower right side of the board.

(5) Adjust the symmetry (SYM) trimmer for a REAL TIME MAGNITUDE reading of zero on the O.M.A. front panel (MAGNITUDE = +00000).

(6) Disconnect the dc supply from TP-1.

6.13D TEST INPUT ADJUSTMENT

After the RAMP, BIAS, and SYMMETRY adjustments are completed, the TEST trimmer is normally set for a REAL TIME, TEST mode input MAGNITUDE = +00100. This setting is convenient for checking the proper function of the O.M.A. console.

6.13E VIDEO OUTPUT ADJUSTMENT

The VIDEO trimmer on the INPUT card is an attenuator control for the VIDEO output on the rear panel of the O.M.A. console. This signal is the analog output of the Detector Assembly after the scan beam chopping, but before A-D conversion. It is provided as a testpoint and to allow the input signal to be viewed while accumulating into the "A" memory. The VIDEO trimmer does not affect the instrument calibration and may be set to any convenient level.

The normal practice is to set the VIDEO trimmer on the INPUT card to provide the same output scale factor (except for dc and time offset) as the REAL TIME mode CRT Y output.

(1) Set the oscilloscope for 50 mV/div, ac coupled. Set the sweep for 50 μs/div, and set the trigger input to trigger the sweep on the positive-going transition of the CURSOR output on the O.M.A. rear panel.

(2) Set the O.M.A. TEST and REAL TIME pushbuttons. Release all remaining pushbuttons. Set SCALE FACTOR = 10^3.

(3) Measure the height of the TEST peak above the baseline level of the CRT Y output on the O.M.A. rear panel (see Figure VI-7).

(4) Connect the scope to the VIDEO output on the O.M.A. rear panel, and adjust the VIDEO trimmer on the INPUT card (#1) for the same test peak height as noted on the CRT Y output (see Figure VI-7).

The VIDEO output signal will have a negative offset whose magnitude will depend on the VIDEO trimmer setting. Note that the VIDEO output is one channel time (64 μs) early due to the time required for digital conversion. This is normal, but it is important to note that if the O.M.A. is set at CHANNEL = 250, the CURSOR output pulse will mark channel 250 at the CRT Y output, and channel 251 at the VIDEO output.

6.14 400 MODE

6.14A DESCRIPTION AND CALIBRATION

The normal operation of the input A-D conversion accepts signals in the −100 to +860 range. This optimizes signal dynamic range while allowing for small accounts of "negative light" due to fluctuations in the dark current and stray light effects on the scan beam chopping process.

The "400 Mode" provides a balanced input mode for applications where the noise level is high, or where significant amounts of light are being imaged on the "dark" half of the vidicon target. In this mode, the input range is

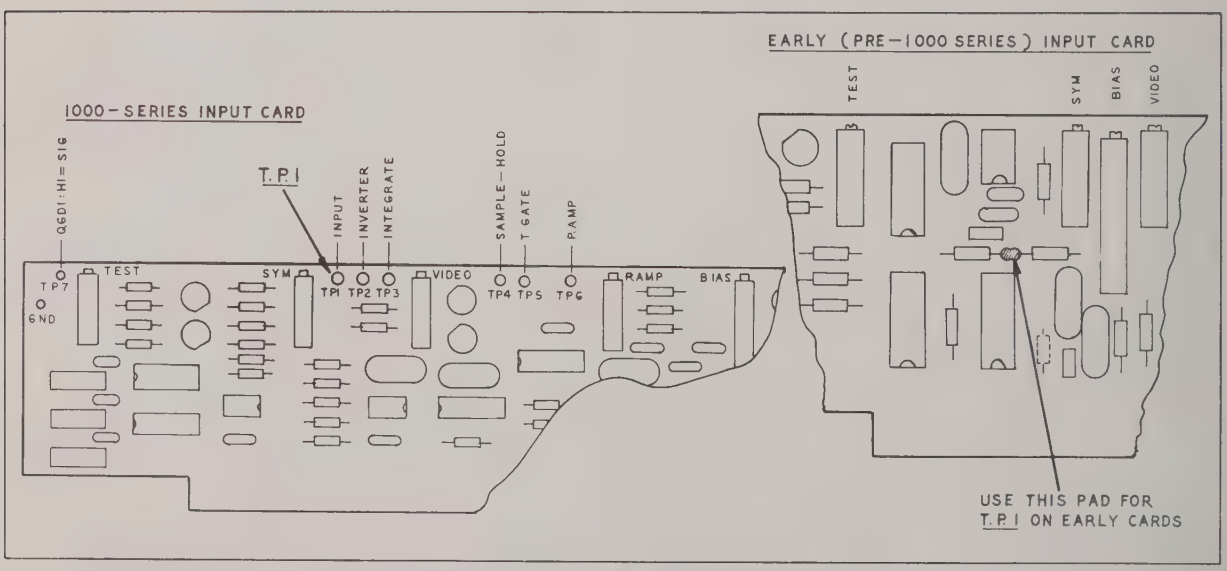


Figure VI-6. TWO VERSIONS OF INPUT CARD

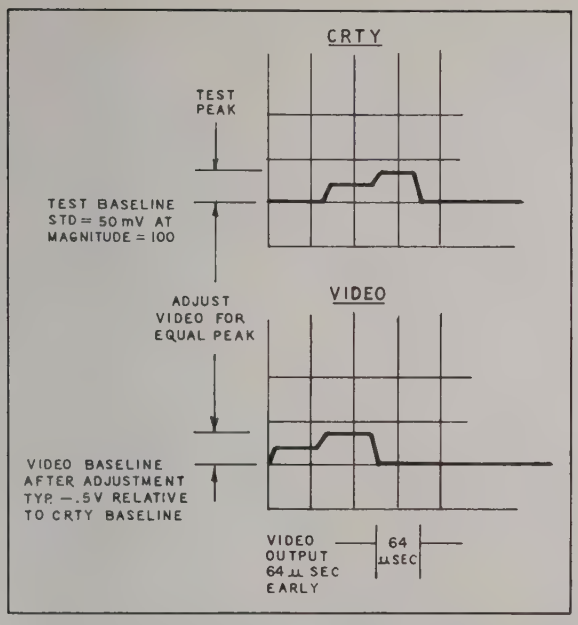

CRTY
TEST PEAK
TEST BASELINE STD = 50 mV AT MAGNITUDE = 100
ADJUST VIDEO FOR EQUAL PEAK
VIDEO
VIDEO BASELINE AFTER ADJUSTMENT TYP. −.5V RELATIVE TO CRTY BASELINE
VIDEO OUTPUT 64 μ SEC EARLY
64 μSEC

Figure VI-7. VIDEO

–400 to +560. The "error light" will come on at +432 and linear overrange will be to +483 in the REAL TIME mode and to +560 in the ACCUM modes.

This mode is controlled by the MEMORY OFFSET switch (S1) at the far right of the TIMING card (#2) and by the setting of the BIAS trimmer on the INPUT card (#1). "400 Mode" calibration is as follows.

(1) Perform the standard INPUT card adjustment as per Section 6.13, with the MEMORY OFFSET switch (S1, TIMING card #2) set in the standard "100" mode position. (S1 to right.)

(2) Set the REAL TIME and TEST pushbuttons. Release all remaining pushbuttons.

(3) Note the MAGNITUDE reading on the O.M.A. front panel.

(4) Set the MEMORY OFFSET switch (S1 on card #2, TIMING card) to the "400" position. (Switch to the left.)

(5) The MAGNITUDE reading should now be 300 counts more negative than that noted in step (3).

(6) Readjust the BIAS trimmer on the INPUT card (#1) to set the MAGNITUDE reading on the value noted in step (3).

(7) When using the "400 Mode", it may be more convenient to calibrate the CRT display for a balanced display presentation as described in Subsection 6.8E.

6.14B RETURNING TO STANDARD MODE

The procedure in the previous subsection (6.14A) may also be used to return the O.M.A. to the standard input mode. In step (4), set the MEMORY OFFSET switch to the right, to the "100" position; this causes the MAGNITUDE reading to go 300 counts more *positive* in step (5).

6.15 PRESET-DELAY REVERSAL

The two switches at the left end of the PRESET card (#9) allow the PRESET and DELAY functions to be interchanged. In this mode, the front panel PRESET switches set the vidion integration delay, while the DELAY switch set the number of cycles in the PRESET HOLD mode. When the vidicon is cooled to dry ice temperatures, this allows the use of delays of up to 9999 ACCUM CYCLES, or about 5½ minutes. Each input cycle will be [(PRESET) + 1] x (32.768 ms) in duration, and a PRESET HOLD measurement will involve (DELAY) input cycles for a total time of ⟦[(PRESET delay) + 1] ACCUM CYCLES/INPUT cycle⟧ x (DELAY input cycles) x (32.768 ms/ACCUM CYCLE).

(1) *O.M.A. POWER must be turned off.*

(2) Set both switches on the PRESET card (#9) to the *left* (←REV←) for the PRESET-DELAY Reverse mode. Set *both* switches to the *right* (→NORM→) for normal O.M.A. operation.

(3) *Check that both switches are in the same position before turning the O.M.A. POWER ON.*

Note that the REMOTE PROGRAM inputs are also exchanged in the PRESET-DELAY Reverse mode. In this mode the sixteen PGMPRExxD1 lines of the PGMPRE16B1 buss are activated by the PREPGMDØ line to set the vidicon integration DELAY, and the four PGMDELxxD1 lines of the PGMDELØ4B1 buss are activated by the DELPGMDØ line to control the PRESET value. See the interface section for details.

6.16 NON-SUBTRACT MODE

The analog subtract switch (S2, ANSUB on the TIMING card, #2) is normally set to the right. When set to the left, it disables the scan beam chopping by turning the detector scanning beam off during the "dark" or subtraction half of each channel scan. If the detector is cooled to reduce the dark current to negligible levels (e.g., dry ice temperatures), this mode allows the detector electronics to be adjusted to scan the entire target area ("light" half + "dark" half) for a signal input. The detector electronics adjustment is covered in Section VIII.

STEP	FUNCTION	SECTION	STANDARD PROC PARA	SET	TEST	ADJUST TRIMMER	CARD #	SET POINT STD
(1)	CRT Display Sweep	6.7	6.7A	HORIZ = CAL	CRT X BNC Output	X RAMP	#7 DISPLAY DRIVER	1.0 volt peak-peak
(2)	CRT Display	6.8	6.8D	SCALE = 10^3, VERT = CAL	CRT Y BNC OUTPUT		#6 OUTPUT	
	(a) reference level			LOG (1)	CRT Y BNC Output	CRT Y Pos'n	---	note output reference level
	(b) LOG Exponent			LOG (1000)	CRT Y BNC Output	EX	#6 OUTPUT	reference plus +300mV
	(c) recheck (a) and (b)							
	(d) LOG Gain (mantissa)			LOG (999)	CRT Y BNC Output	LOG-G	#6 OUTPUT	reference plus +300mV as for LOG (1000)
	(e)Linear Zero Position			Linear (000)	CRT Y BNC Output	POS	#6 OUTPUT	equal to reference level in (a)
	(f) FULL Scale			Linear (999)	CRT Y BNC Output	LIN G	#6 OUTPUT	reference plus +500mV
(3)	CRT Display Intensity (cursor makk)	6.9	6.9A	HORIZ = CAL CHANNEL = 499 scope trig. on CURSOR	CRT Z BNC Output		#7 DISPLAY DRIVER	
	(a) LEVEL					L	"	+400 millivolts
	(b) BLANK					B	"	-200 millivolts
	(c) MARK (cursor)					M	"	+900 millivolts
	(d) COMPENSATE expanded brightness			HORIZ = full clockwise		C	"	+200 mV shift in CRT Z (L = .6V, M = 1.1V, B = 0V)
(4)	Plotter Sweep	6.12		PLOT/PRINT	PLOT X BNC Output	PLOT RAMP	#7 DISPLAY DRIVER	10 millivolts/second ramp rate
	(a) reference ramp method:		6.12D	TEST trim CCW BIAS = +200 PLOT RATE = 6 DELAY = 5 PRESET = 499 Erase A Cursor zero TEST, PRESET HOLD, Display select "A"				
				PLOT/PRINT + A ACCUM	PLOT X minus PLOT Y	PLOT RAMP	#7 DISPLAY DRIVER	zero change in difference voltage
(5)	INPUT Card	6.13					#1	
	(a) RAMP (A-D calibrate)		6.13A	-----	TP6, input card	RAMP	#1 INPUT	10.0 volts peak-peak
	(b) BIAS (zero input level)		6.13B	TEST trim CCW REAL TIME TEST	front panel MAGNITUDE reading	BIAS	#1 INPUT	MAGNITUDE = +00000
	(c) SYMMETRY *****		6.13C	release TEST				
				disconnect Detector Assy set REAL TIME				
				Apply small DC voltage @ TP1, INPUT card.	front panel MAGNITUDE reading			MAGNITUDE = +00000 ± 2
	(d) TEST	6.13D		TEST REAL TIME	MAGNITUDE reading	TEST	#1 INPUT	MAGNITUDE = +00100

Table VI-2. SUMMARY OF ADJUSTMENT PROCEDURES AND PARAMETERS

SECTION VII
USE OF NON-STANDARD DISPLAY SCOPES

7.1 GENERAL DISCUSSION

The O.M.A. is designed to operate with a CRT display that is dc-coupled, that has a 100 mV/division X and Y-axis input sensitivity, an 8 x 10 division display area, and a dc-coupled, 0 to +1 V, positive-intensity, Z-axis input. Calibration of the instrument to this display, or to any other X-Y-Z display with reasonably similar parameters is covered in SECTION VI.

If a standard display is not available, the O.M.A. can be adapted for use with a wide variety of non-standard displays, including most general purpose oscilloscopes. The most common problem areas are lack of a sufficient X-axis (horizontal) input sensitivity and lack of a sensitive Z-axis input for the cursor channel marker. This section suggests a number of alternate approaches, in some cases with some loss of operator convenience.

The next three subsections are a listing of some of the display application alternatives, with reference to detailed information in later subsections.

7.1A NON-STANDARD X-AXIS (SWEEP)

AC-Coupled X-axis inputs may be used, but a level shift will occur when the O.M.A.'s HORIZ DISPLAY EXPAND mode is used. This will require readjustment of the display's horizontal position control whenever the display expansion is changed.

Low Sensitivity X-axis inputs may be accommodated by a modification of the DISPLAY DRIVE card. This is normally not recommended, as problems can develop with the use of the resulting non-standard instrument with standard displays. See Subsection 7.9.

Dual Trace Oscilloscopes often have a second X-axis mode in which one of the vertical input amplifiers may be used to drive the X-axis at the O.M.A. standard of 100 mV/division. This often operates via the one-channel internal trigger controls. Refer to the manual for the particular instrument.

Triggered Sweep may be used, but will require the operation of two controls for display expansion: the oscilloscope time base will provide expansion while the CAL - non-CAL setting of the O.M.A. HORIZ EXPAND control will set a normal or cursor-centered display. See Subsection 7.2.

7.1B NON-STANDARD Y-AXIS (VERTICAL)

DC-Coupled Only. AC coupled vertical inputs will cause incorrect display, particularly with signals involving input to all 500 channels (e.g., the spectrum of an incandescent lamp).

Minimum Slew Rate. In order to produce a satisfactory display, the CRT beam must be capable of being displaced the full height of the display in less than 10 μs. Most displays with a vertical bandwidth of 100 kHz will be adequate in this respect, however, a vertical bandwidth of 500 kHz or more is preferable for optimum display appearance.

Sensitivity. Most standard scopes provide either a 100 mV/division range or a 1.0 V full scale range. The O.M.A. can be calibrated to accommodate either of the above, or any display where a usable display presentation will result from a signal in the range of ±0.35 V full scale to ±0.8 V full scale. It is only necessary to identify the required calibration points on the display device in terms of O.M.A. output values, and the calibration may be performed by the procedure in Subsections 6.8C and 6.8D of the preceding section.

Low Sensitivity. The linear O.M.A. output modes (but not the LOG mode) may be expanded to up to ±2.0 V full scale by use of the front panel O.M.A. control VERT DISPLAY EXPAND. If this is done, the lack of detent to allow return to the calibrated intermediate setting will prevent the use of the O.M.A. control for vertical scale expansion. Normally, only the on-screen portion of the CRT display receives linear expansion; the CRT Y output is designed to limit at over ±2 V to prevent input overload in the standard display. Thus, only partial display expansion may be used to compensate for limited display sensitivity unless the O.M.A. is modified as described in Subsection 7.9. This modification will allow the O.M.A. to be calibrated at up to ±5 V full scale in the full clockwise position of the VERT SCALE EXPAND control. This modification is normally not recommended as it eliminates the LOG and scale expand features, and will result in improper operation when the modified O.M.A. is used with a normal CRT display. The display appearance will be degraded on large magnitude signal peaks, due to the slew rate limitations of the CRT Y output driver.

Non-Standard Graticule. Any CRT display graticule scheme is usable if the signal levels are appropriate to the CRT Y output capability. Reference to the standard display elsewhere in the manual should be taken to refer to the corresponding CHANNEL and MAGNITUDE values on the actual display used. Some oscilloscopes have a limited vertical graticule area such as 3, 4, or 6 by 10 divisions. In these cases it may be desirable to set up the O.M.A. so that the negative portion of the normal display is off the screen, since this area is not significant in most applications. If the graticule is 10 x 10 divisions square, the balanced display calibration described in Subsection 6.8E may be preferable to the standard display pattern.

7.1C Z-AXIS (INTENSITY) AND THE CURSOR

The "Z" (intensity) axis is not required for proper presentation of the 500 channels of signal information. The primary function of the Z axis is to improve operator convenience by providing an intensified marker of the channel selected for digital output. A number of alternate approaches to this requirement are available. The secondary

functions of the Z-axis are retained when possible. They are: (1) Blanking the ACCUM CYCLES counter and unused channels so that they will not be incorrectly identified as signal channels. The blank gap also serves to identify the transition from channel 499 to channel 000 when the expand mode places this in the middle of the screen. (2) The "glitches" as the D-A converter goes from one channel to the next are blanked. This is an appearance matter unless the display is being viewed by a secondary sensor which cannot ignore interchannel spiking as the human eye can. (3) The O.M.A. corrects the display brightness as the expand mode is used, thus saving the operator the necessity of operating a second control.

The basic cursor methods available are as follows.

Sensitive Z-Axis Inputs. Z-axis inputs requiring only a few volts to control the display brightness may be accommodated by the standard use of the CRT Z output or the CRT Z HIGH output, as described in Subsections 6.9 and 6.10. CRT Z HIGH is used if more than +2 V is required, or if the input requires a negative-going voltage to intensify the display. Note that these inputs are often identified by the maximum allowable non-damaging input. Thus an input identified as "Z-axis, ±15 V max." often operates directly from the 1 V standard CRT Z output.

Blanking Inputs. Blanking inputs usually require the use of the CRT Z HIGH output to invert the standard output waveform. See Subsection 6.10.

AC Cathode Blanking. Most older general-purpose oscilloscopes have this input, requiring up to 60 V to blank the beam. In most cases the CRT Z HIGH output will provide a usable cursor marker with these inputs. With careful adjustment it is often possible to retain most of the blanking functions as well, at the expense of a second intensified dot at channel ØØØ due to the ac coupling. See Subsection 7.3.

Dual Trace Oscilloscopes. The CURSOR output on the O.M.A. rear panel provides a 64 μs, +5 V pulse during the selected channel time. Viewed on the second input of a dual-trace scope, it provides a marker pip that points at the selected channel.

Dual Time Base Oscilloscopes. The "B intensified by A" mode of many dual timebase oscilloscopes can be set up to provide an intensified cursor marker. See Subsection 7.6. Display expansion is usually somewhat less convenient in this mode as it requires the use of a triggered sweep mode instead of the usual horizontal input from CRT X.

Trace Switching. Some display scopes, particularly digital storage scopes, have a Z-axis input which switches the trace on and off, with no intermediate intensities. The O.M.A. Z-axis can be adjusted to provide the usual interchannel and retrace blanking with these displays. When the O.M.A. is given full horizontal expansion, the blanking will allow the individual channels to be counted, and the cursor-selected channel will be the twelfth channel from the left on the display. See Subsection 7.7.

Operator Technique. If none of the above methods is suitable, the operator can locate the cursor-selected channel by taking advantage of the operating characteristics of the O.M.A. See Subsection 7.8.

7.2 TRIGGERED SWEEP DISPLAYS

7.2A SETUP

The following procedure will set up a triggered oscilloscope to use triggered sweep instead of the X (horizontal) axis input.

(1) Set the O.M.A. HORIZ DISPLAY EXPAND to the CAL position.

(2) Connect the oscilloscope to the CRT X output of the O.M.A. (32.8 ms sawtooth) and adjust the X RAMP trimmer (card #7, DISPLAY DRIVER) for an amplitude sufficient to provide a stable external trigger input to the display scope.

(3) Connect CRT X to the external trigger input of the display scope. Set the scope to trigger on a negative going transition of its external trigger input, and set the time base for a rate faster than 32.8 ms (2 ms/div typical).

(4) Set the O.M.A. TEST and REAL TIME pushbuttons and set SCALE FACTOR = 10^3. Set the cursor for CHANNEL = 000.

(5) If the O.M.A. vertical outputs have been set up, examine the test peak on CRT Y. If not, connect the scope to view the CURSOR output pulse (+5 V, 64 μs pulse), and adjust the variable ("uncalibrated") time base control on the scope until the display shows exactly one 32.8 ms cycle on the screen.

(6) Connect the scope vertical to CRT Y and adjust.

7.2B OPERATION

Connected as above, the scope will produce a 500-channel scan, with channel 000 at the left. If there is no scope blanking, the retrace blank and ACCUM CYCLES counter region will be visible just to the left of channel 000, and should be ignored. Display expansion is achieved as follows.

(1) Turn the O.M.A. HORIZ DISPLAY EXPAND slightly clockwise, out of the CAL position. This alters the triggering so that the cursor channel will always be the twelfth channel after the trigger.

(2) Expand the display by increasing the oscilloscope sweep speed. Readjust the intensity control as necessary.

(3) Return to the standard presentation by reversing the process above.

7.3 HIGH-LEVEL, AC-COUPLED Z AXIS

The following adjustment procedure calls for viewing the Z-axis drive waveform on an oscilloscope while adjusting and observing its effect on the display scope intensity. If a second scope is not available, it is possible to alternate between the two oscilloscope functions. In the procedure, "scope" refers to the examination of signals with an oscilloscope, while "display" will refer to the oscilloscope set up for use with the O.M.A.

(1) Set up the O.M.A. as follows.

HORIZ DISPLAY EXPAND: CAL
"A" DISPLAY SELECT: set
remaining pushbuttons: released
CURSOR: CHANNEL = 250
"A" MEMORY: erased

(2) Connect the scope to the CRT Z output and connect the scope trigger to the CURSOR output. Set the scope for 200 μs/div and 500 mV/div, and adjust for trigger stability.

(3) Adjust the LEVEL ("L"), BLANK ("B") and MARK ("M") trimmers on card #7 (DISPLAY DRIVER) for the CRT Z waveform shown in Figure VII-1a.

(a) Set ("L") for −500 mV LEVEL.

(b) Set ("B") for −1.0 V BLANK LEVEL.

(c) Set ("M") for +500 mV MARK pulse.

(4) Set the scope for 5.0 V/div and connect to the CRT Z HIGH output.

(5) Set the "HIGH" switch (at right edge of card #7, DISPLAY DRIVER) to the left (to the "−" position).

(6) Adjust the CRT Z HIGH trimmer ("H", just to the left of the switch on card #7, DISPLAY DRIVER) fully counterclockwise.

(7) While observing the CRT Z HIGH waveform, turn the CRT Z HIGH trimmer ("H") clockwise. The waveform will increase in amplitude and shift level in a positive direction. When the waveform reaches the circuit limit at about +13 V, further adjustment will reduce the difference between the LEVEL and BLANK levels on the signal. Stop adjusting the trimmer when the LEVEL and BLANK potentials just become equal, resulting in the waveform shown in Figure VII-1b.

(8) Connect the CRT Z HIGH output to the display set up for the 500-channel unexpanded display. Adjust the display intensity for a moderate baseline brightness.

(9) There should be an intensified dot in the middle of the screen, at the channel 250 position. If not, set the "HIGH" switch to the right, to the "+" position. One of the two switch positions should produce an intensified dot. If not, the CRT Z HIGH circuit may not have sufficient drive for the display.

(10) If both positions appear to produce an intensified dot, temporarily connect the display vertical input to the CRT Z output. The correct "HIGH" switch setting is the one that produces a bright spot *above* the baseline.

(11) If the "HIGH" switch is set to the "+" position to achieve an intensified spot, repeat steps (6) and (7), adjusting for the waveform shown in Figure VII-1c. Note that the waveform will appear to be correct without readjustment, but the trimmer setting will be wrong.

(12) While observing the intensified dot on the display, adjust the MARK trimmer ("M", card #7, DISPLAY DRIVER) counterclockwise. The set point is the *minimum* setting that will produce an acceptable marker dot. The higher (more CW) the setting, the greater will be the tendency for the marker to extend into the next channel due to the slew rate limitations of the CRT Z HIGH circuit. With some high level displays, the best display appearance may require a fairly low basic baseline brightness.

(13) Connect the scope to the CRT Z HIGH output and examine the amplitude of the cursor peak. If the peak is 8 V or less in amplitude, the following steps will provide the blanking and expanded mode brightness compensation functions. If the peak amplitude is 10 V or more, the remaining steps in this procedure may not significantly improve the display appearance. Should this prove to be the case, refer to Subsection 7.4 - LOW SENSITIVITY Z AXIS.

(14) Set the O.M.A. cursor to CHANNEL = 470, and set the HORIZ DISPLAY EXPAND control just slightly clockwise from the CAL position. In this uncalibrated but not greatly expanded condition the cursor dot will be near the left edge of the screen, and the retrace blank region (between CHANNEL 499 and CHANNEL ØØØ) will be about 1/3 division wide, about one division from the left of the screen. The retrace region will *not* be blanked at this time.

(15) Adjust the LEVEL trimmer ("L") on the DISPLAY DRIVER card (#7) clockwise. At the same time, turn the display's brightness control down as necessary to maintain the original baseline brightness. Continue these adjustments until the retrace interval mentioned in step (14) is blanked (Figure VII-1d). This will normally result in an additional intensified region at channel ØØØ (just to the right of the blank), due to the recovery of the ac coupling after the long (12 channel times) retrace blanking interval.

(16) Set the COMPENSATE trimmer ("C", card #7, DISPLAY DRIVER) fully counterclockwise.

(17) (Skip this step if using a triggered-sweep display instead of the X-axis of an X-Y display.) Turn the HORIZ DISPLAY EXPAND control fully clockwise for a fully expanded display. Adjust the COMPENSATE trimmer ("C") clockwise to produce a usable display brightness.

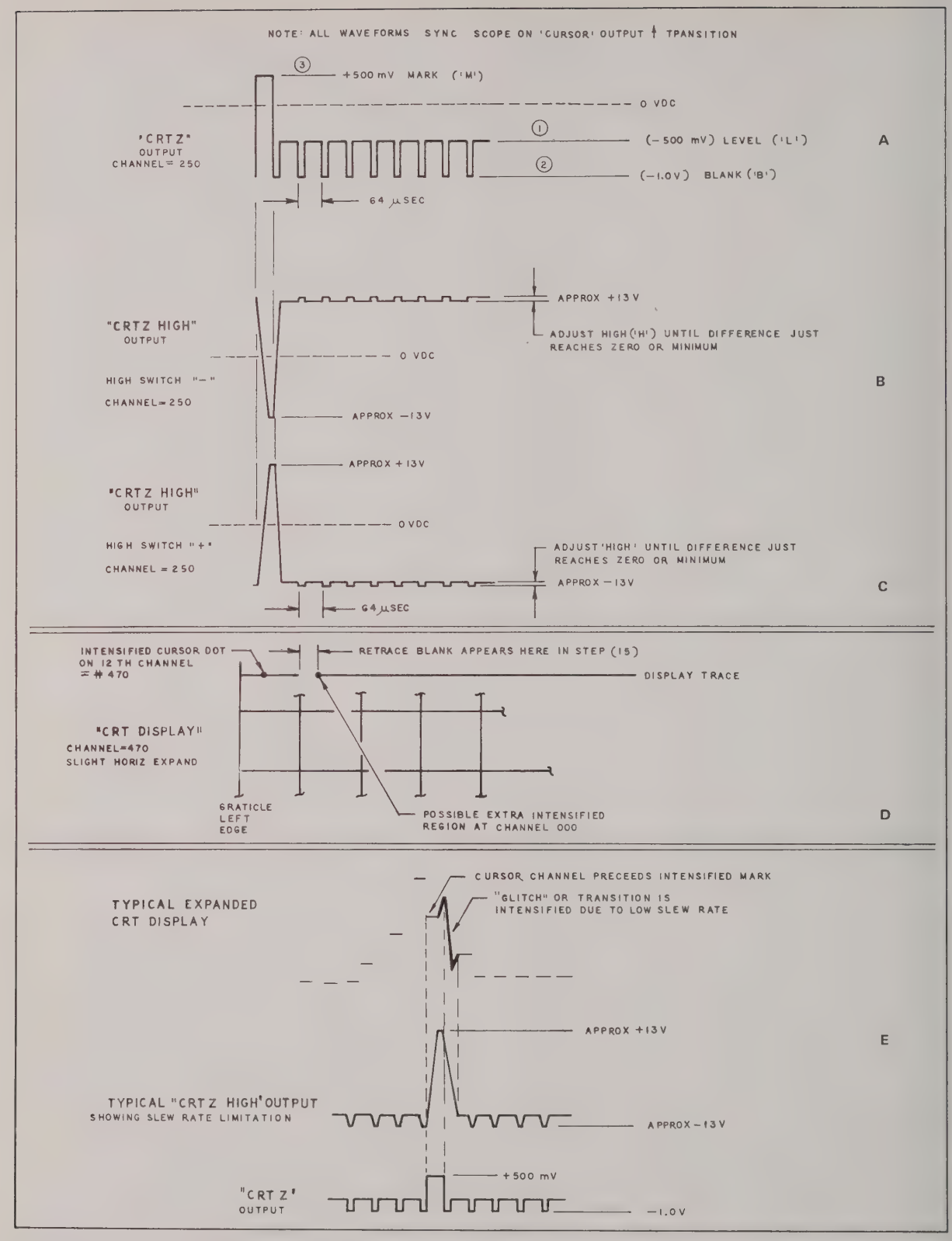

NOTE: ALL WAVEFORMS SYNC SCOPE ON 'CURSOR' OUTPUT ↑ TPANSITION
③ +500 mV MARK ('M')
0 VDC
"CRTZ" OUTPUT CHANNEL = 250
① (-500 mV) LEVEL ('L')
② (-1.0V) BLANK ('B')
A
64 μSEC
APPROX +13V
"CRTZ HIGH" OUTPUT
ADJUST HIGH('H') UNTIL DIFFERENCE JUST REACHES ZERO OR MINIMUM
0 VDC
HIGH SWITCH "-" CHANNEL = 250
APPROX -13V
B
APPROX +13V
"CRTZ HIGH" OUTPUT
0 VDC
HIGH SWITCH "+" CHANNEL = 250
ADJUST 'HIGH' UNTIL DIFFERENCE JUST REACHES ZERO OR MINIMUM
APPROX -13V
C
64 μSEC
INTENSIFIED CURSOR DOT ON 12 TH CHANNEL = # 470
RETRACE BLANK APPEARS HERE IN STEP (15)
DISPLAY TRACE
"CRT DISPLAY" CHANNEL=470 SLIGHT HORIZ EXPAND
GRATICLE LEFT EDGE
POSSIBLE EXTRA INTENSIFIED REGION AT CHANNEL 000
D
CURSOR CHANNEL PRECEEDS INTENSIFIED MARK
TYPICAL EXPANDED CRT DISPLAY
"GLITCH" OR TRANSITION IS INTENSIFIED DUE TO LOW SLEW RATE
APPROX +13V
E
TYPICAL "CRTZ HIGH" OUTPUT SHOWING SLEW RATE LIMITATION
APPROX -13V
+500 mV
"CRTZ" OUTPUT
-1.0V

Figure VII-1. CRT DISPLAY DRIVE WAVEFORMS

Step (15) will increase the demands on the slew rate of the CRT Z HIGH output circuit. The lower the sensitivity of the display Z-axis input, the more noticeable the effect of a slew rate on the display appearance. When the Z-axis sensitivity is low, step (15) or step (17) may reduce the quality of the cursor dot to unusable levels. If these steps have an unfavorable effect on display appearance, they should not be included in the setup procedure.

When the display Z-axis input sensitivity is low, the effect of the slew rate limitation is to cause the intensifying cursor pulse to appear late (Figure VII-1e). In extreme cases, the intensified dot will include the transition between the selected channel and the next channel. The marker will appear as an intensified or illuminated spike or transition between two channels on the display. In this case, the cursor-selected channel (appearing in the numeric display) will be the channel *before* or to the left of the intensified transition.

7.4 LOW SENSITIVITY Z-AXIS

The O.M.A. setup for low sensitivity Z-axis inputs is covered in Subsection 6.10 for dc inputs, and in Subsection 7.3 for ac inputs. In some cases, however, the Z-axis input sensitivity is such that the O.M.A. CRT Z HIGH output cannot provide the full range of mark, blank, and compensate levels required. The procedure in this paragraph maximizes the output for cursor marker intensification. If this will not produce a satisfactory cursor dot, one of the alternate cursor schemes must be used (see Subsection 7.1C).

(1) Perform steps (1) through (7) in Subsection 7.3. However, in step (3b), set the BLANK trimmer ("B") fully counterclockwise. The BLANK level will be about –600 mV, and is not critical.

(2) Set up the display for the 500-channel, unexpanded display. Adjust the display intensity for a moderate baseline brightness. Then connect the display intensity input to the O.M.A.'s CRT Z HIGH output.

(3) Switch the "HIGH" switch on the DISPLAY DRIVER card between the "+" position and the "–" position.

(a) If the baseline brightness remains constant and either position results in an intensified dot in the middle of the display, perform steps (9) through (12) in Subsection 7.3. This is the characteristic of an ac-coupled Z-axis input.

(b) If the baseline brightness in the two switch positions differs (or if one position blanks the display), steps (4) through (8) below should be followed. This is the characteristic of a dc-coupled Z-axis input.

(c) It may be necessary to reduce the display intensity setting to observe either effect (a) or (b). If the Z-axis input sensitivity is very low, use of a scope hood and a very low basic brightness level may allow a usable cursor dot contrast with the CRT Z HIGH output levels available.

(d) If neither effect (a) nor (b) can be observed, the CRT Z HIGH output has insufficient drive to provide a cursor marker, and one of the alternate marker schemes must be used. However, it may prove worthwhile to check for a defective CRT Z HIGH output or display Z-axis input.

(4) If (3b) is observed, set the "HIGH" switch to the position that produces the dimmer or blanked baseline.

(5) If the base line is blanked, turn up the display brightness control as necessary to produce a visible baseline. If setting the display brightness control for maximum brightness fails to produce a visible baseline, turn the O.M.A.'s LEVEL trimmer ("L") clockwise until a baseline is visible at the maximum brightness setting of the display.

(6) The display should now show an intensified dot in the middle of the baseline at CHANNEL 250. If this dot is too bright, turn the O.M.A.'s LEVEL trimmer ("L") clockwise to increase the baseline brightness, and then reduce the display brightness control setting to return to the original baseline brightness with a dimmer cursor dot.

(7) When a satisfactory display is achieved in step (6), turn the O.M.A. POWER switch OFF. This will normally result in a single bright spot on the display screen. If so, turn the POWER back on and proceed to step (8). If no bright spot is observed:

(a) Turn up the display's brightness control until a bright spot is observed, and then turn the control down until the spot is just barely extinguished.

(b) Turn the O.M.A. power ON.

(c) Turn the O.M.A. LEVEL trimmer clockwise to produce the desired baseline brightness.

(d) Turn the O.M.A.'s MARK trimmer ("M") counterclockwise to reduce the cursor dot to the desired brightness.

(8) Observe the CRT Z HIGH output waveform on an oscilloscope. Note the amplitude of the cursor marker peak. Turn the O.M.A.'s MARK trimmer ("M") counterclockwise until the magnitude of the marker pulse is observed to decrease slightly. Then turn the MARK trimmer clockwise just enough to return the cursor marker peak to the level originally noted.

When the adjustment of the CRT Z HIGH output is completed, examine the resulting output waveform with an oscilloscope. If the cursor marker peak is 10 V or less in magnitude, there is a good possibility that the procedure of Subsection 6.10 (dc Z-axis inputs) or the rest of Subsection 7.3 (for ac-coupled inputs, steps 12 through 17) may result in improved display appearance.

7.5 DISPLAY BURNOUT PRECAUTIONS

Note that the O.M.A. settings described for use with ac-coupled Z-axis inputs or low sensitivity Z-axis inputs may be such that the display will have a bright spot on the screen when the O.M.A. power is turned off. If this is the case, there is the possibility of display damage due to prolonged, overbright exposure of a single spot on the display CRT. Operating both instruments from outlets with a common power switch is recommended in this case.

7.6 DUAL TIME BASE CURSOR

The following procedure will allow the "B intensified by A" mode of many dual-time-base general-purpose oscilloscopes to be used to provide the intensified cursor marker. The method does require that the scope be used in the triggered sweep mode, with the resulting loss of convenience when horizontal scale expansion is desired. The setup is as follows.

(1) Set up the "B" or delaying time base for external triggering on the negative-going transition of a positive waveform (the CRT X sawtooth).

(2) Connect the "B" trigger input to the CRT X output on the O.M.A. rear panel.

(3) Adjust the "B" or delaying time base sweep rate and triggering for a stable display of at least one complete O.M.A. output scan. Temporarily connecting the display vertical input to the CRT X or CURSOR output will provide a convenient means of checking this setting. If the CURSOR output is used, set the cursor for CHANNEL = ØØØ. If the "B" time base has a vernier control, slowing the time base from a setting of 2 ms/div will provide an optimum display of the 32.8 ms/scan O.M.A. output.

(4) Set the DELAY TIME MULTIPLIER or vernier delay control for zero delay between the "B" time base and "A" time base.

(5) Set the "A" or delayed time base for externally triggered operation on a positive-going transition of a positive pulse (the CURSOR pulse). Set the "A" sweep rate to 5 μs/div.

(6) Connect the "A" or delayed time base trigger input to the CURSOR output on the O.M.A. rear panel.

(7) Set the oscilloscope for "B INTENSIFIED BY A" operation.

(8) Move the O.M.A. cursor to CHANNEL = 250.

(9) Adjust the oscilloscope intensity and "A" time base triggering to obtain a stable intensified dot in the middle of the display area. When the "A" triggering is correctly set, the intensified dot will follow the cursor position right and left as the O.M.A. CHANNEL number increases and decreases.

(10) Check that the "A" or delayed time base is triggering on the positive-going transition of the CURSOR output. This may be done by temporarily connecting the scope vertical input to the CURSOR output (along with the "A" trigger) to check that the intensified dot is on top of the +5 V CURSOR pulse, or by checking the REAL TIME, 10^3, TEST mode O.M.A. display for a cursor dot and test peak as shown in Figure III-1. If the "A" time base is triggering on a negative-going transition, the intensified dot will be on the channel following the desired channel.

7.6A DUAL TIME BASE OPERATION

When set up as above, Display expansion is achieved by turning the O.M.A.'s HORIZ DISPLAY EXPAND control slightly clockwise, out of the CAL position. This will alter the triggering so that the cursor-selected channel will be the twelfth channel from the left edge of the display. The "B" or delaying time base sweep rate control may then be changed to expand the display. When the HORIZ DISPLAY EXPAND control is returned to the CAL position, and the scope sweep rate is returned to the original setting, the display will again be arranged with channel ØØØ at the left and channel 499 at the right.

Because of the use of the triggered sweep mode, and the lack of a display blanking input, the frame retrace interval and ACCUM CYCLES counter region will be visible at the left edge of the screen in the CAL or normal display, and between CHANNEL ØØØ and CHANNEL 499 (if on the screen) in the expanded mode. These regions combined involve 12 channels (500 to 511) or 768 μs on the display. Care should be taken to avoid interpreting these channels as signal channels.

Some dual timebase scopes lack a sweep vernier in the "B" timebase. With these scopes it will be necessary to use a slower sweep speed, such as 5 m/div in step 7.6(3) and to use a reduced length or multiple display. That is, there will be about 1½ complete scans on the screen, and in some cases a scope control will allow the trace to be shortened to blank the extra 1/2 scan.

7.7 TRACE SWITCHING DISPLAYS

Some CRT displays, particularly digital storage displays, have a switching or two-state Z-axis. These scopes allow the beam to be turned on or off, but provide no intermediate brightness level control. These displays cannot provide an intensified cursor marker, but can provide the retrace and interchannel blanking functions. This allows the cursor-selected channel to be conveniently identified in the full horizontal expand mode, by counting twelve channels from the left edge of the display.

7.7A BLANKING-NORMAL SETUP

To set up the O.M.A. outputs for a digitally controlled Z-axis scope, the on and off levels required by the display should be identified by referring to the manual for the display device. If the required signal is in the ±1 V range, with the ON level the more positive voltage, the CRT Z output can be used directly. The setup is as follows.

(1) Turn the MARK trimmer fully counterclockwise. (Trimmer "M", DISPLAY DRIVER, card #7.)

(2) Observe the CRT Z output on an oscilloscope. Adjust the LEVEL trimmer ("L", DISPLAY DRIVER card) to set the more positive output level at the desired display ON voltage.

(3) Adjust the BLANK trimmer ("B", DISPLAY DRIVER card) to set the more negative CRT Z output level to the appropriate display OFF voltage level.

7.7B BLANKING; LOW SENSITIVITY SETUP

If the required Z-axis signal is positive-blanking or requires levels greater than ±1 V, the CRT Z HIGH output must be used. The CRT Z output is adjusted for a negative-blanking signal with voltages about one-tenth the desired levels. The CRT Z HIGH trimmer and switch are then set for the desired signal amplitude and polarity at the CRT Z HIGH output.

For example, suppose the required signal levels are –9 V = ON, +1 V = OFF. The procedure would be as follows (all adjustment points are on the DISPLAY DRIVER card).

(1) Set the MARK trimmer ("M") fully counterclockwise.

(2) Set the LEVEL trimmer ("L") for +0.9 V for the most positive level on the CRT Z output. (Note that the CRT Z levels are set as though for a positive-ON, negative-OFF signal).

(3) Set the BLANK trimmer ("B") for –0.1 V for the more negative level on the CRT Z output.

(4) Set the CRT Z HIGH switch ("HIGH") to the "–" position (to the left) to invert the signal at the CRT Z HIGH output.

(5) Adjust the CRT Z HIGH trimmer ("H") so that the ON level of the CRT Z HIGH output is at the desired level (–9 V in the example).

(6) Readjust the BLANK trimmer ("B") as necessary to produce the desired OFF signal level at the CRT Z HIGH output.

(7) It may be necessary to touch up the settings of the LEVEL and BLANK trimmers after the display is connected to the CRT Z HIGH output, to correct for loading characteristics of the display input.

7.8 NO CURSOR MARKER

There are two basic methods of identifying the cursor position on the CRT display in the absence of any of the cursor-marking methods discussed in the preceding paragraphs.

The first method relies on the fact that the cursor-selected channel is always the 12th channel from the left of the display when in the horizontal display expand mode. If the display position controls are adjusted so that this channel is over a graticule line when the O.M.A.'s HORIZ DISPLAY EXPAND control is in the fully clockwise position, the desired channel will always be located over this line when the display is so expanded. If necessary, a special graticule line may be applied to the display screen for this purpose.

The second method takes advantage of the characteristics of the TEST mode O.M.A. input. When the O.M.A. is set for TEST, SCALE FACTOR = 10^3, and REAL TIME, there will be an artificial test peak in the two channels following the cursor-selected CHANNEL. This may be used to identify the general position of the cursor on the unexpanded display, or to mark the cursor channel location on the display screen in the expanded mode. The channel selected for digital display will be in the same horizontal position when the O.M.A. is switched back to a signal input or memory display mode. Note that this method must not be used during a signal accumulation, as the TEST signal will be added to the detector signal already accumulated.

7.9 HIGH OUTPUT MODIFICATIONS

It is possible to increase the CRT X and PLOT X output drive capabilities somewhat by modification of the DISPLAY DRIVER card. These modifications are normally not recommended for the following reasons: (1) either modification will cause improper operation when the O.M.A. is used with a standard display; and (2) non-standard cards cause extra problems should repair of the instrument become necessary, because known good cards cannot be exchanged for suspect cards. For these reasons, *modification tags must be attached both to the modified card(s) and to theO.M.A.* to avoid non-warranty repair charges.

7.9A HIGH OUTPUT CRT X (SWEEP) MODIFICATION

The CRT X modifications involve C14, ZD1, and R36 on the DISPLAY DRIVER card #7. These components are located near the middle of the card, just below and to the right of the X RAMP trimmer (see Figure VII-2).

(1) Remove ZD1 from the DISPLAY DRIVER card.

(2) Remove R36 from the DISPLAY DRIVER card.

(3) Replace the 0.1 μF mylar capacitor, C14, with a 0.01 μF capacitor. This will allow the X RAMP trimmer to be set for up to +12 V full-scale horizontal deflection ramp at the CRT X output.

(4) Select and install an appropriate zener diode at ZD1. The diode is installed with the cathode band down, toward the connector edge of the card.

When the O.M.A.'s HORIZ DISPLAY EXPAND control is turned to the expand position, the CRT X output ramp rate is increased by up to a factor of ten, and the peak ramp voltage is similarly increased unless it is limited by the +12 V output limit of the CRT X op. amp, or by ZD1.

ZD1 is selected to clamp the expanded CRT X output at a level greater than the full-scale deflection require-

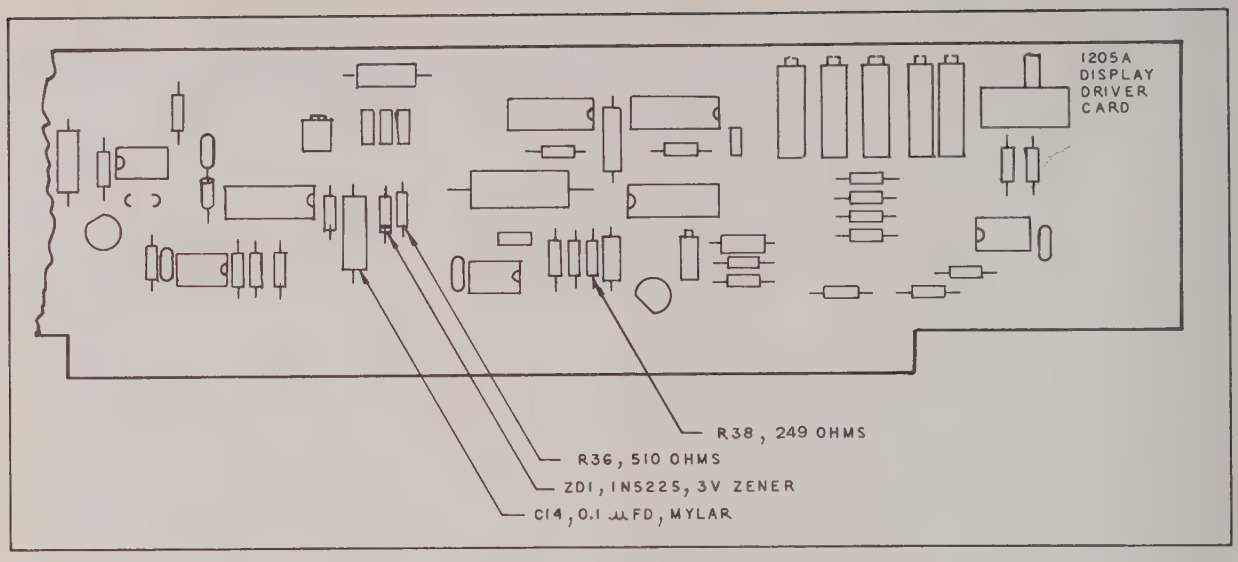


Figure VII-2. DISPLAY DRIVER CARD

ment of the display, but low enough to prevent overloading or saturation of the display input. ZD1 is not required if the display deflection requires 10 - 12 V.

If the display deflection requirement is less, select a zener diode with a nominal voltage about 2 V greater than the full scale deflection voltage (e.g., Standard 100 mV/div display full scale = 10 div. or 1.0 V. Standard ZD1 is 3 V, 1N5225).

(5) Attach a modification tag or label to the card.

(6) Replace the card in the O.M.A. and adjust X RAMP to the display as described in Subsection 6.7B.

Note that the modified CRT X output may still be adjusted to operate a standard 100 mV/div display when the O.M.A. HORIZ DISPLAY EXPAND control is set to the CAL position. However, horizontal expansion will result in severe overload or saturation of the display input. This usually appears as severe distortion of the display image as the degree of expansion is increased.

7.9B HIGH OUTPUT PLOT X MODIFICATION

Disconnecting either end of R38 on the DISPLAY DRIVER card will increase the PLOT X ramp rate range and maximum output by a factor of six, allowing up to +12 V output to drive the plotter sweep. R38 is a 249 ohm, 1% resistor located near the middle of the DISPLAY DRIVER card, just to the left of the PLOT RAMP trimmer. See Figure VII-2 and the DISPLAY DRIVER card schematic. Note that the PLOT X output impedance is increased appreciably by this modification.

SECTION VIII
ADJUSTMENT OF DETECTOR HEAD ELECTRONICS

8.1 PRELIMINARY

Adjustment of the Detector Assembly drive electronics requires that the 1205A console be calibrated and set up with a suitable CRT display, as described in Sections VI and VII. The adjustment of the electronic focus requires a focused or high-contrast optical signal on the signal or "light" half of the detector target. A single point of light is convenient for this purpose, as it avoids interaction between the electronic focus adjustment effects and the effects of the optical alignment of the input image discussed in Subsection 4.5 - OPTICAL INPUT ALIGNMENT. Other signal formats such as one or more properly aligned and focused spectrometer slit images are also usable for adjusting the electronic focus. If neither the electronics nor the optics are exactly focused, it is still possible in most cases to achieve a correct setting by observing the CRT display and alternately "peaking" the electronic and optical adjustments until the correct combined adjustment is reached.

> **NOTE**
>
> The figures in this section are idealized sketches intended to illustrate specific operating characteristics. Actual operation of the instrument may not duplicate the figures. However, the desired adjustment normally is readily identified by the "peaking" or optimization of the characteristic indicated in the figure.

The procedure in the following paragraphs covers the alignment of the 1205A electronics for use with the 1205B, 1205E, 1205F, and 1205G. The procedures for other detector assemblies are generally similar, but may differ in detail or in the basic adjustment levels used. These differences are covered in application notes for the specific detector assembly.

8.2 RECORDING SETTINGS

Table VIII-1 shows the preliminary settings for the detector head electronics. Additional space is provided on this table to record settings derived for special applications or additional detectors. It is strongly recommended that the existing settings of the detector head electronics be recorded before attempting any readjustment. If an adjustment other than that derived at the factory is used, this also should be recorded. This provides initial settings for recalibration and/or replacement of these cards, as well as providing needed reference information for troubleshooting this portion of the instrument.

CIRCUITRY CHECKED	SETTING OR LEVEL
POWER SUPPLY	
+15V	+15 V ±0.5 V
-15 V	-15 V ±0.5 V
+5 V	+5 V ±0.1 V
HIGH VOLTAGE CARD	
G1	-70.0 V
G4	+340 V
G3	+290 V
G2	+300 V
BLANK, ALIGN, AND FOCUS CARD	
L. ALN	0.0 V
F. ALN	0.0 V
FOC. I	
Relative to -15V	3.8 V
Relative to GND	-11.2 V
CATH	-6.0 V
FRAME SCAN CARD, TP-1	
F. POSN	0 V
F. SCAN	8.2 V pk-pk
LINE SCAN CARD, TP-2	
L. POSN	
Switch	CEN.
Trimmer	Fully CCW
L. SCAN	7.5 V pk-pk
INPUT CARD, TP-6	
RAMP	10.0 V pk-pk
DETECTOR PREAMP	
R2, TP-1	Min. DC
R10	Fully CCW

Table VIII-1. PRELIMINARY SETTINGS

8.3 INITIAL O.M.A. SETUP

The adjustments in this section are performed in the REAL TIME mode. The initial setup is as follows.

REAL TIME: set
remaining pushbuttons: released
SCALE FACTOR: 10^3
DELAY: 0
DISPLAY EXPAND
HORIZ: CAL
VERT: CAL

8.4 SAFETY PRECAUTIONS

(1) HIGH VOLTAGES are present within the 1205A console and the detector assemblies.

(2) INTENSIFIED DETECTOR assemblies (1205D, etc.) must be protected against excessive input light before applying power.

(3) Care is required in handling the signal/power connectors on the 1205A and detector assemblies. Do not stand the detector assembly on its connector end. Do not use force in inserting either end of the detector assembly signal/power cable. When the connectors are correctly aligned, only a few ounces pressure are required to overcome friction in the retaining clips.

(4) The detector faceplate is fragile and is accessible at the front of the unmounted detector assembly. A plastic cap is provided for faceplate protection. For proper operation the faceplate must be kept free of dust, lint, fingerprints, etc. Metal objects near the 1205D faceplate can cause arcing through the faceplate, which in turn will cause tube failure.

8.5 INITIAL SETTINGS: 1205B, F, & G

The following initial settings are approximately correct for the 1205B, 1205E, 1205F and 1205G detector assemblies. The final optimum values are reached by the adjustment sequence in the following paragraphs. The initial voltages are set using the testpoints and adjustment trimmers indicated in Figure VIII-1. All voltages are measured with a high impedance meter (10 MΩ or higher). The fram scan, line scan, and cathode voltage (target voltage) adjustments require an oscilloscope. Testpoints for these signals are also available on the vidicon filter board located under the rear cap of the detector assembly. The G2 voltage may be slightly less on the vidicon filter board due to voltage drop in the filter.

8.5A HIGH VOLTAGE CARD

Perform the following adjustments in the order indicated. The G2 and G3 voltages are partially dependent on the G1 and G4 settings, and any adjustment of G1 or G4 will require readjustment of G2 and G3.

G1 = −70 V
G4 = +340 V
G3 = +290 V
G2 = +300 V

8.5B CONNECT DETECTOR ASSEMBLY

Connect the detector assembly to the console at this time, if this has not already been done. Recheck the settings just completed in Subsection 8.5A.

8.5C BLANK, ALIGN & FOCUS CARD

The L. ALN and F. ALN trimmers are initially set for zero volts. The initial zero volt settings may be measured on the console POWER/SIGNAL output connector pin 14 (L. ALN) and pin 15 (F. ALN). Any non-zero value is affected by the coil loading: predetermined non-zero F. ALN and L. ALN settings must be made with the detector assembly connected, using the left end of the 240 Ω resistors on the BLANKING, ALIGNMENT, & FOCUS cards.

LA = 0.0 V dc
FA = 0.0 V dc

The *focus current* (FOC 1) is set to 38 mA, indicated by +3.8 V difference between the focus current testpoint (B, A, & F card TP-1) and the −15 V supply. Connect the (+) meter lead to TP-1 and the (−) lead to −15 V. The focus current is 10 mA per indicated volt.

FOC 1 = 38 mA = +3.8 V { (+) → TP-1 ; (−) → −15 V supply }

Note that the −15 V supply is regulated at some voltage in the range of −14.5 V to −15.5 V. The focus current testpoint (TP-1) is set 3.8 V more positive than this or between −10.7 V and −11.7 V relative to the O.M.A. ground.

The vidicon target voltage is determined by the negative level of the cathode signal. This is the VCATHAN signal indicated in Figure VIII-1, and may be viewed on an oscilloscope connected to the CATH testpoint (TP-2) next to the CATH trimmer on the Blank, Align, & Focus card. If the non-subtract mode has been selected by setting S2 on the TIMING card to the left, this signal will be a 64 μs square wave instead of the waveform shown. In either case, the CATH trimmer is adjusted for −6.0 V peak negative level, as indicated in the figure.

CATH = −6.0 V negative peak at TP-2

If this testpoint shows a +15 V level that does not respond to the CATH trimmer, the scan protection blanking circuit is probably active. Check for at least 3 V pk-pk at the frame scan testpoint and at the line scan testpoint TP-2. Adjust the F. SCAN and L. SCAN trimmers as necessary to exceed these minimums and activate the VCATHAN signal at the CATH testpoint.

8.5D FRAME SCAN CARD

Connect the oscilloscope to the Frame Scan testpoint and observe the 32.8 ms scan waveform. Adjust the F. SCAN trimmer for 8.2 V pk-pk amplitude, not including the spikes at the retrace transition. Adjust the F. POSN trimmer for zero dc offset, i.e., equal positive and negative peak values, *not* including the retrace spike. See Figure VIII-1.

F. SCAN = 8.2 V pk-pk
F. POSN = zero dc
} at frame-scan testpoint, spikes not included.

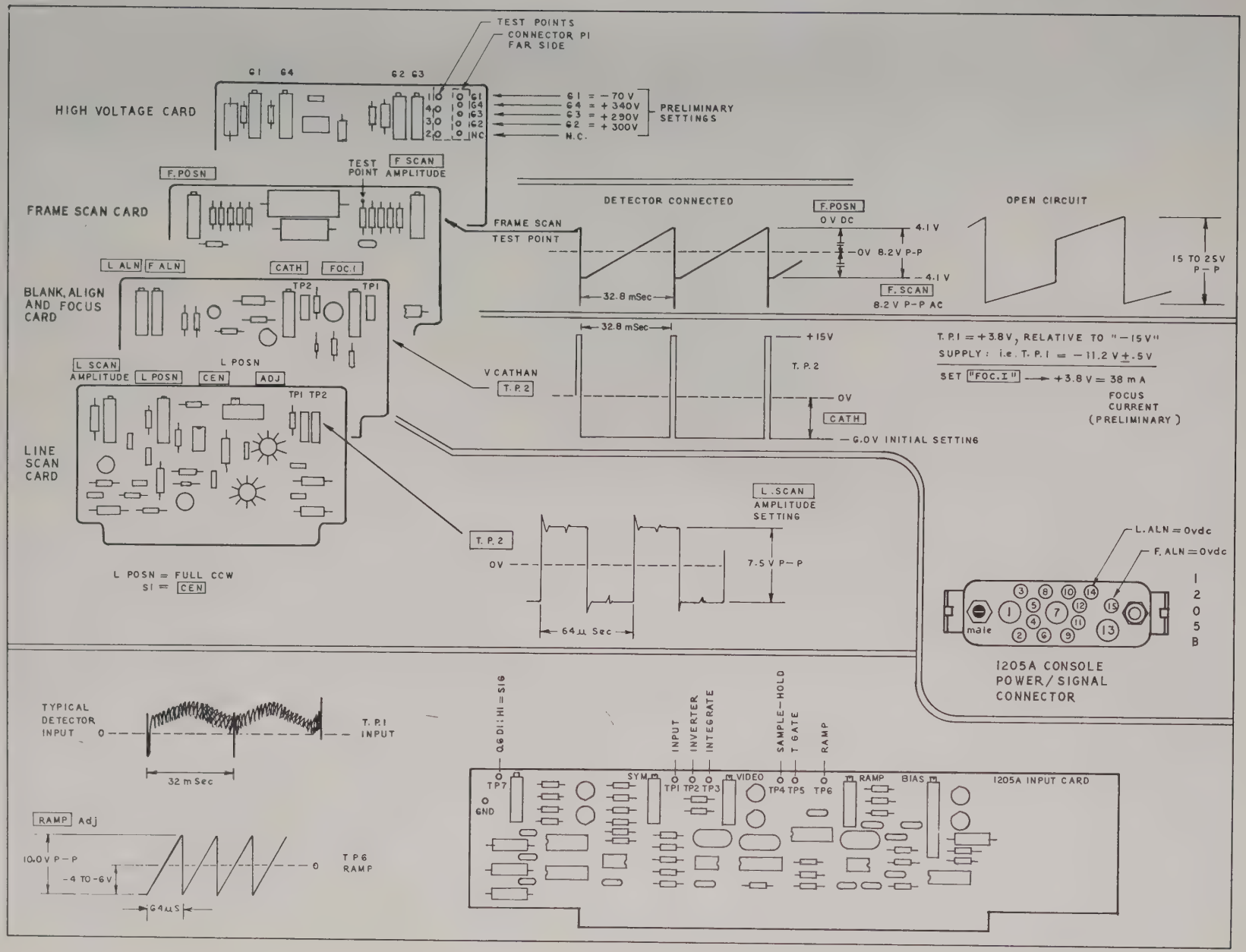


Figure VIII-1. TESTPOINTS AND INITIAL VALUES

8.5E LINE SCAN CARD

The switch on the Line Scan Card is set to the left, the CEN position. The L. POSN trimmer is set fully counterclockwise (indicated by clicking at the end of travel). The L. SCAN trimmer is set for the correct scan amplitude as follows: Connect the oscilloscope to TP-2 on the line scan card and observe the 64 μs square-wave output signal (see Figure VIII-1). Adjust the L. SCAN trimmer for 7.5 V pk-pk amplitude of the basic square wave, ignoring the small spikes at the leading edge and midpoint of each half cycle.

L. POSN = fully counterclockwise
Switch = CEN (to the left)
L. SCAN = 7.5 V pk-pk at TP-2, not including spikes.

8.5F PREAMPLIFIER

The Vidicon Preamplifier board is located in the rectangular shielding box on the side of the Detector Assembly. Remove the cover (eight screws) and set the two trimmers as follows: Cover the detector or optical instrument input so that no light falls on the detector target. Measure the voltage at the testpoint (next to trimmers - see Figure VIII-2), and adjust the OFFSET ADJ trimmer R2 to minimize the voltage at the testpoint. Set the second trimmer, R10 to the fully counterclockwise position.

R2 = minimum dc at testpoint, dark
R10 = fully counterclockwise

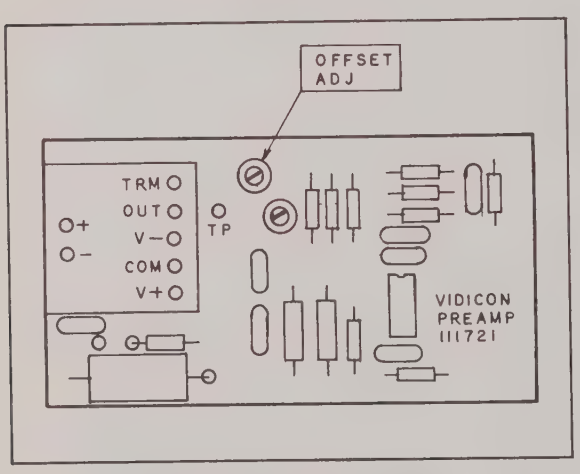


Figure VIII-2. VIDICON PREAMP

Examine the 32.8 ms input signal cycle at TP-1 on the INPUT card in the O.M.A. console. (A typical waveform is shown in Figure VIII-1.) Ignore the large signal spikes occurring during the retrace interval (every 32.8 ms) and note the level of the ac signal from the 500 signal channels. If these show a large positive offset (most negative peaks at +3 V to +5 V, positive peaks approaching +8 V to +10 V), adjust R10 slightly clockwise until most of the signal is near zero on the negative peaks. If the input is very negative, or −13 V, R10 is probably not set to the proper CCW position.

Replace the preamp cover and detector assembly rear cap before continuing with the adjustment procedure.

8.6 OPERATION CHECK

With the Detector covered so that no light falls on the target, examine the real time O.M.A. output on the CRT display. Two effects should be observed: random noise, verifying proper operation of the preamp; and baseline curvature, indicating proper operation of the vidicon. The VERT DISPLAY EXPAND control may be used to make these effects more visible.

If either effect is missing, check the following.

(1) Is the console in the correct output mode, Subsection 8.3?

(2) Is light leaking onto the detector?

(3) Is there an input limit condition, indicated by a constant CRT and numeric display magnitude either exactly −100 or greater than +780? The positive limit is also indicated by the "error light" in the numeric display window. In either case the BIAS trimmer on the INPUT card should be readjusted as necessary to bring the CRT display baseline into the zero to +100 MAGNITUDE region. CW = (+), CCW = (−).

(4) If random noise with no baseline curvature is observed, turn the CATH trimmer on the Blank, Align, & Focus card clockwise until CRT display baseline curvature appears. This increases the target voltage (CATH testpoint goes more negative than original −6.0 V setting).

Optical inputs on the vidicon faceplate should now produce positive or negative-going signals on the CRT display. Note that small regular spikes or bumps traveling from left to right across the display are not the random noise described above. These are normally the result of incomplete alignment at this point, or a lack of proper shielding (i.e., missing preamp cover or detector assembly rear cover, or the lack of a properly-shielded input device to prevent noise pickup at the vidicon target).

8.7 ADJUSTMENT PROCEDURE

8.7A OPTICAL SIGNAL REQUIRED

At this point, the adjustment procedure requires an optically focused light spot or slit image on the signal portion of the detector target. Preferably the spot or slit image should be less than .001" (25 μm) or one channel wide. A slit image must be aligned with the scan pattern as discussed in Subsection 4.5. Using a spot for initial alignment requires only focus and placement of the spot somewhere in the "signal" or "light" half of the detector target scan area. If necessary, this optical alignment and focus may be approximately set by analysis of the detector scan and mounting dimensions in Figure II-1. Final alignment and focus may then be found by alternately peaking the electronic and optical adjustments. Non-signal light must be eliminated or minimized, to avoid limiting the vidicon preamplifier. This condition is satisfied if noise and baseline curvature are still evident as described in Subsection 8.6.

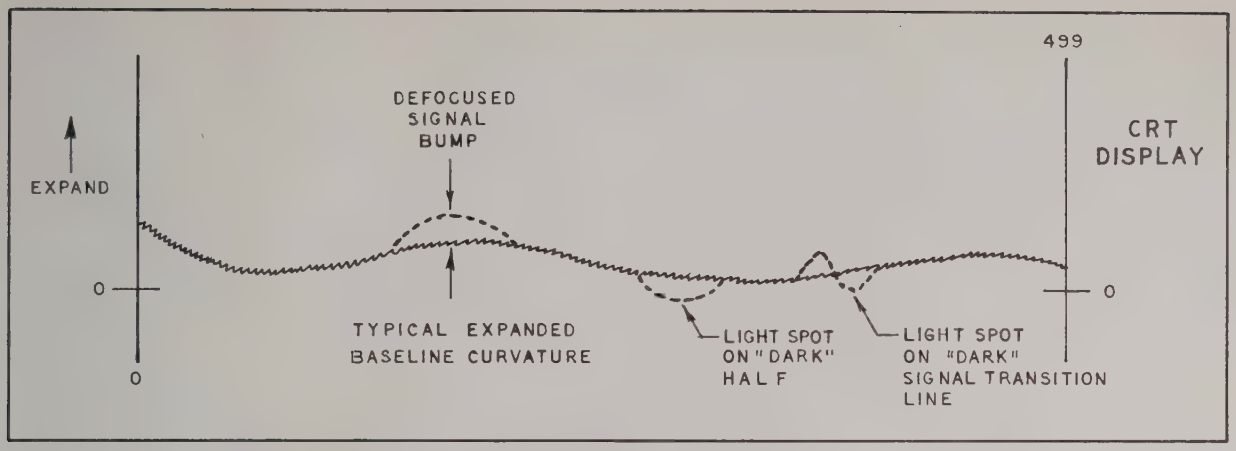


Figure VIII-3. LOCATING SIGNAL PEAK

8.7B LOCATING THE SIGNAL PEAK

The signal described in the previous paragraph should produce a peak or bump on the O.M.A. CRT display baseline. This may be from 2 to 50 or more channels wide, depending on the amount of additional focusing required. If the input signal is being spread into many channels, it may be necessary to increase the input intensity (using caution with intensified detectors such as the 1205D) or to rapidly vary the input light intensity or position on the target to locate the corresponding signal output on the REAL TIME CRT display. If the signal appears as a dip or up-and-down wave in the display baseline, the light is probably falling on the "dark" or "subtract" area of the target. Refer to Subsection 4.5 and Figure II-1. The O.M.A. VERT DISPLAY EXPAND control may help make the signal bump visible. Once the output signal is located, the focusing adjustment may proceed.

8.7C FOCUS AND PARAMETER OPTIMIZATION

Optical and electronic focusing are carried out by maximizing the amplitude and minimizing the width of the positive-going peak observed on the CRT display. If the spot or slit image is several channels wide, the middle channels will indicate about the same intensity regardless of focus. In this case the focus is adjusted to optimize the sharpness at the edges of the peak. As the focus is improved, the top of the peak will become wider and the base narrower, until in the ideal (but impossible) situation all channels would be either at the peak or on the baseline with none in between.

There will be some crosstalk that will spread some of the signal from a single channel input into the adjacent channels. Consider a single channel input such as a spectral line image of a 25 micron slit, focused and aligned on a single channel detector element. Because the crosstalk spreads some signal into the adjacent channels on either side, the number of channels in the peak cannot be reduced to less than three. Slight rotation or focus errors appear as extra crosstalk rather than as extra channels in the peak. The final adjustment of focus and rotation is for minimum apparent crosstalk, i.e., maximum center channel magnitude and minimum side channel magnitude.

Each of the following adjustments has an optimum setting such that adjustment to either side will degrade the performance. As the focus adjustment proceeds, the input light intensity must be readjusted whenever necessary to prevent an input signal limit condition on the peak channel indicated by the "error light" in the numeric display window, and by a peak MAGNITUDE greater than +732. If the input image is a spot, local detector saturation is also possible, indicated by the peak refusing to rise above some level (less than +732) as the intensity is increased. In this case the input intensity must be reduced until the peak is observed to fall significantly below this level. The adjustment procedure follows.

(1) *Adjust Optics* per Subsection 4.5. Note that if the input is a slit image, rotational alignment of the slit image with the detector channel elements is quite critical.

(2) *Adjust the focus current - FOC. I.* trimmer on the Blank, Align, & Focus card. Set for optimum focus.

(3) Repeat steps (1) and (2) until no further improvement is noted.

(4) Adjust G1, the vidicon control grid voltage trimmer on the HIGH VOLTAGE card in the following manner: Adjust the input light intensity for an O.M.A. CRT display peak that is near the limit level, but low enough to respond to a small increase in input intensity. Then adjust the G1 trimmer negatively (counterclockwise) until the peak height on the CRT display begins to decrease. *Set G1 clockwise +10 V (approx. 1 turn CW) from the fall-off point.*

(5) Set the vidicon target voltage. This is determined by the negative level on the VCATHAN signal observed at the CATH testpoint (TP-2) on the BLANK, ALIGN, & FOCUS card. Observing a near-saturation peak on the CRT display as in step (4) above, turn the CATH

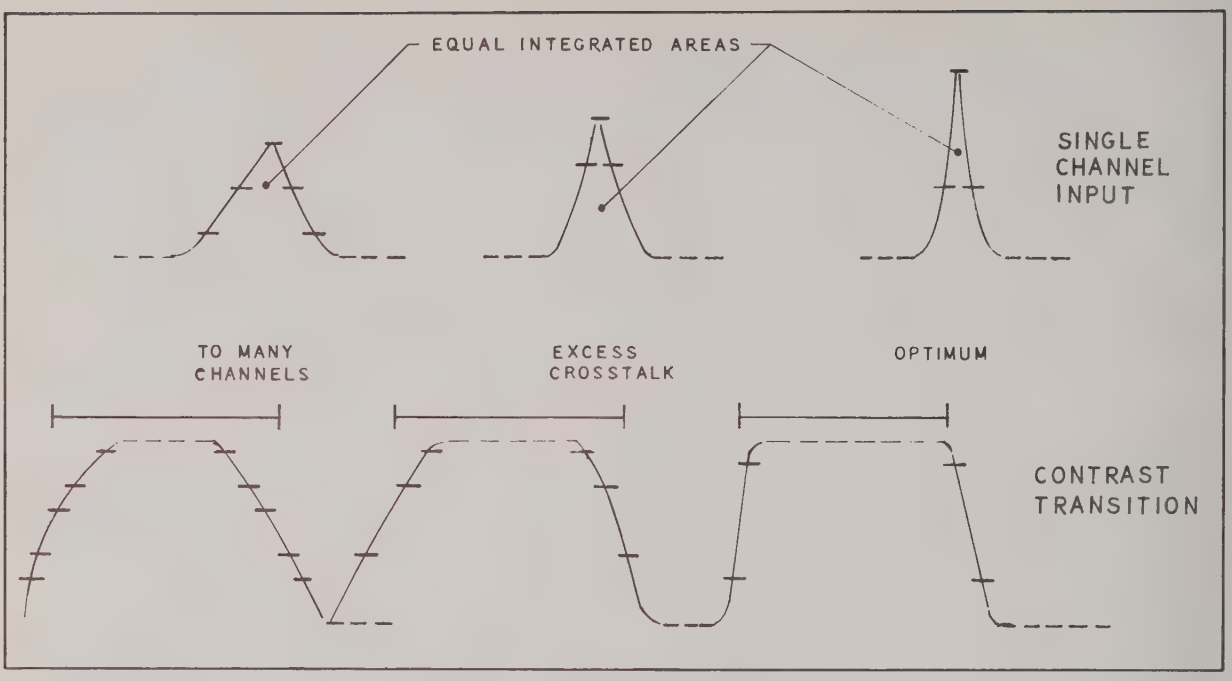


Figure VIII-4. FOCUSING AND CROSSTALK

trimmer counterclockwise (positive) until the peak height on the CRT display begins to decrease. Turn the CATH trimmer back 2 volts more negative (approx. 2 turns clockwise) from the fall-off level. Setting the cathode voltage more negative reduces target lag (Subsection 4.6C), but increases dark current and defect structure.

(6) Repeat steps (1) and (2) to peak up the focus and current (FOC. 1) settings. For optimum performance, *keep the input image centered* on one channel as discussed in Subsection 8.9 - FINE TUNING.

(7) *Adjust the F. ALN trimmer* on the BLANK, ALIGN, & FOCUS card as follows (see Figure VIII-5).

(a) An input signal is required that will provide a focused image at each end of the detector scan at about channels 050 and 450. Figure VIII-5a shows a portion of the mercury spectrum from a fluorescent lamp, applied through the standard P.A.R.C. #1206 Polychromator, but the adjustment may be performed by moving the input signal used in the earlier steps from one end of the detector to the other from time to time as necessary.

(b) Position the O.M.A. cursor just to the left of the right-hand peak (see Figure VIII-5a) and turn the O.M.A. HORIZ DISPLAY EXPAND control clockwise so that both peaks are expanded but still on the display, as in Figure VIII-5b.

(c) *Measure and record the negative voltage level of the VCATHAN waveform* at the CATH testpoint TP-2 on the BLANK, ALIGN, & FOCUS card.

(d) Turn the *CATH trimmer counterclockwise* until one or both of the signal peaks become defocused on the CRT display (Figure VIII-5c or e).

(e) *Adjust F. ALN until both peaks are sharp* (Figure VIII-5d). If the input source only provides one signal peak, it will be necessary to shift the input from about channel 50 to about channel 450 while gradually adjusting F. ALN. When the F. ALN setting is incorrect the focus will favor one or the other end of the detector (Figure VIII-5c and e).

(f) Repeat steps (d) and (e) until the optimum F. ALN setting is reached.

(g) Readjúst the CATH trimmer on the BLANK, ALIGN, & FOCUS card to return the negative level of the VCATHAN waveform to the level noted in step (c).

(8) *Adjust the L. ALN trimmer.* If the input device permits a point of light to be positioned at the top or bottom ends of the detector channel element, then the L. ALN adjustment may be made by the method used for the F. ALN setting. That is, reduce the target voltage (CATH setting) to defocus, and adjust L. ALN so that neither the "light" (positive peak) nor the "dark" (negative peak) half of the target is more defocused. Note that the limit conditions previously mentioned must be prevented. It may be necessary to

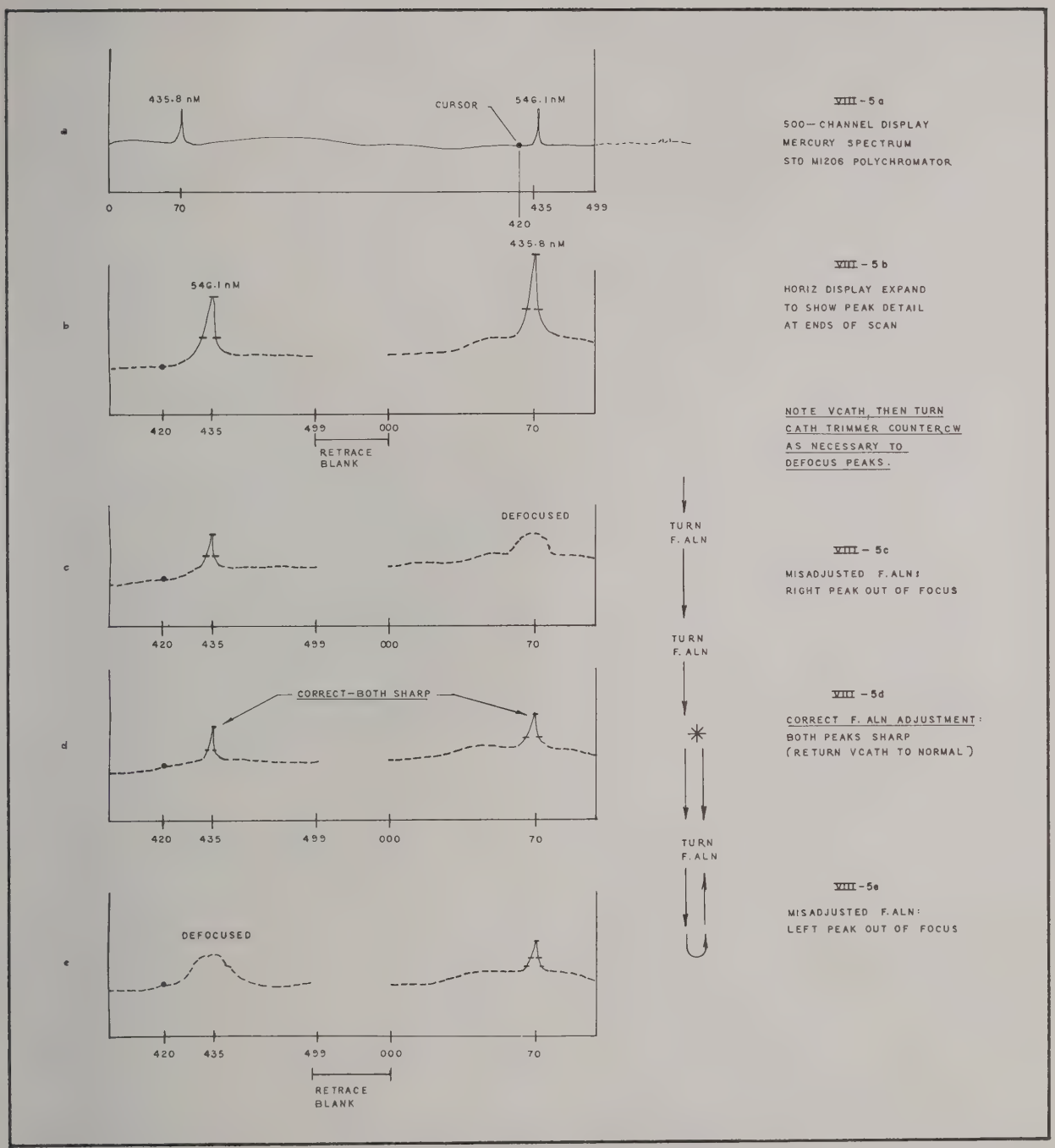


Figure VIII-5. L. ALN AND F. ALN ADJUSTMENTS

turn up the BIAS trimmer to avoid a limit at −100 on the "dark'. or background subtract peak.

If the necessary optical input signal for this procedure is not available, and the input is a slit image, the L. ALN trimmer may be adjusted by the same procedure used to set F. ALN in step (7). The two adjustments will interact, and the desired setting of both L. ALN and F. ALN is that which produces the best focus at high and low channel numbers.

(9) *Adjust the SYMMETRY* trimmer on the *INPUT card.* Cover the detector so that no light falls on the detector target, and examine the dark current baseline and curvature. Change the O.M.A. front panel DELAY setting from Ø to 1 to 2. As the DELAY setting is increased, the magnitude of the baseline curvature will increase, and the average position of the baseline will change. Adjust the symmetry trimmer to *minimize the shift* in the baseline position as the DELAY setting is changed. Only slight readjustment from the standard

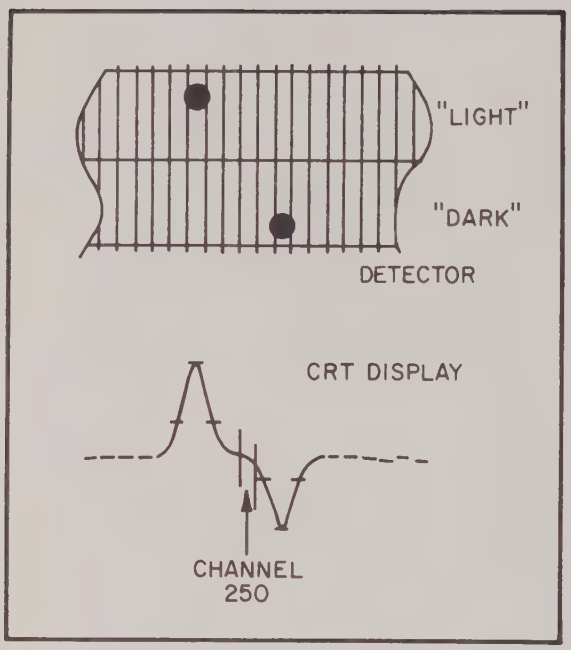


Figure VIII-6. L. ALN ADJUSTMENT

setting (Subsection 6.13C) should be required. In some cases the symmetry setting that eliminates the shift between DELAY = Ø and DELAY = 1 will increase the shift between DELAY = 1 and DELAY = 2 in such a way that the shifting cannot be entirely eliminated. This indicates that the shift is not due to scan or dark current symmetry effects. Some improvement may be realized by rechecking the preamp, L. ALN, and F. ALN adjustments, but the optimum setting of the symmetry (SYM) trimmer in this case will usually be the standard adjustment covered in Subsection 6.13C.

(10) Adjust the BIAS trimmer on the INPUT card so that the dark current baseline is at zero. This adjustment is made with no light on the detector target, and DELAY = Ø. The baseline curvature will prevent setting all channels at zero. Choose the setting that places most of the baseline either at zero or just slightly positive.

(11) *Reset the TEST mode.* Set the TEST pushbutton on the O.M.A. front panel, and adjust the TEST trimmer on the INPUT card to the desired TEST mode input signal magnitude (usually MAGNITUDE = +1ØØ). Release the TEST pushbutton.

8.8 CALIBRATION

8.8A FRAME SCAN/WAVELENGTH

The O.M.A. frame scan characteristics may be more exactly calibrated if a suitable reference signal is available. For example, the standard P.A.R.C. Model 1206 Polychromator provides a dispersion of 3.02 Angstroms per channel when set up with the 600 g/mm grating and 135 mm lens. In the sketch, the distinctive mercury vapor lines from a standard fluorescent lamp are used to calibrate the O.M.A. frame scan amplitude to this exact dispersion.

Note that turning F. SCAN counterclockwise will expand the spectrum by reducing the size of the detector scan pattern. This does not increase resolution, which is already near the limit allowed by the characteristics of the detector. Setting F. SCAN too far CCW will only reduce the available spectral range. Setting the F. SCAN control too far clockwise will eventually cause the scan pattern to extend beyond the useful area of the vidicon target, providing a small increase in spectral range at the expense of a large loss of performance in the end channels. This usually appears as a loss of sensitivity in the edge channels and a large non-uniformity in the ends of the dark current baseline.

8.8B FRAME POSITION/OPTICAL AXIS

A known input signal allows the F. POSN trimmer to be set exactly to align detector channel 250 with the optical axis of the input device. In the example of the previous subsection, the Model 1206 Polychromator is aligned so that the center wavelength is indicated on the instrument's WAVELENGTH scale. Fine tuning in this adjustment, or alignment of the O.M.A. scan pattern, is accomplished after the frame scan calibration is complete by setting the Polychromator for a known wavelength (e.g., 5461 A) and adjusting the O.M.A. F. POSN trimmer slightly to position the corresponding CRT display peak over CHANNEL 25Ø. Turning F. POSN clockwise moves the CRT display peak toward CHANNEL ØØØ. Note that moving the F. POSN trimmer too far from the original zero setting may move one end or the other of the detector scan off the useful target area, causing the symptoms mentioned in the previous subsection.

8.8C RAMP/SENSITIVITY

The setting of the RAMP trimmer on the INPUT card controls the conversion ratio of the input analog-to-digital converter. If a suitable standard light source is available it may be used in conjunction with this control to calibrate the O.M.A. or to standardize the performance of two or more O.M.A.'s. Note that quantum efficiency and other effects vary with wavelength and with different detectors. Thus any calibration is only valid at the specific reference wavelength. The degree of mismatch at other wavelengths will depend on the spectral bandwidth covered and the response characteristics of the individual detectors.

The most convenient reference source is a single-slit image properly aligned and centered on one detector channel element. The slit image should be shorter than the 0.2" channel element so that all of the light will fall on the active area of the target. The wavelength and intensity must be known. This pattern will allow all but the final fine adjustment to be performed quickly in the O.M.A. REAL TIME MODE. Turning the RAMP trimmer counterclockwise will increase the apparent magnitude of the peak on both the numeric and CRT displays.

Optimum accuracy is obtained after a final adjustment to standardize the net integrated signal in the display peak.

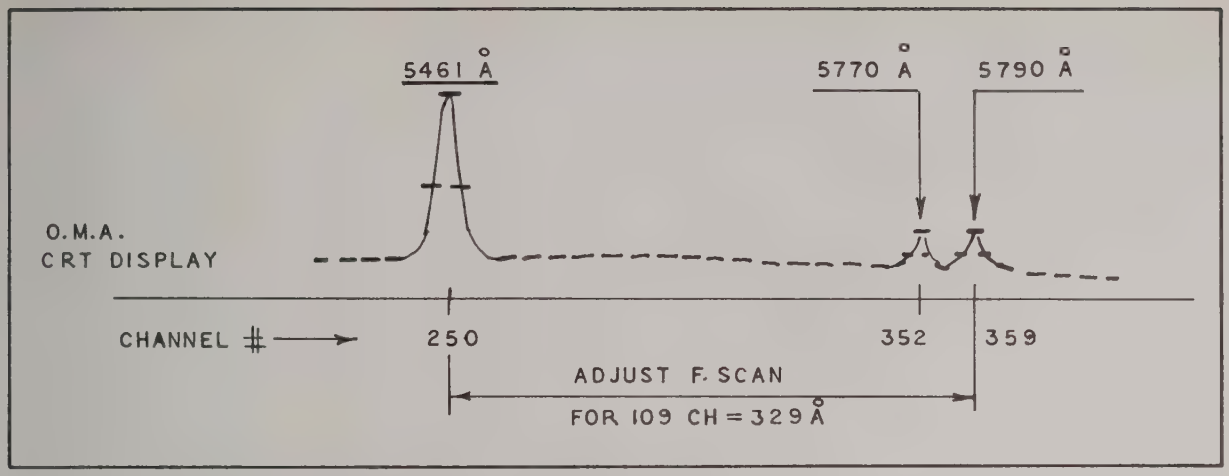


Figure VIII-7. FRAME SCAN/WAVELENGTH CALIBRATION WITH MODEL 1206 POLYCHROMATOR SET TO 5461 A CENTER WAVELENGTH (600 g/mm GRATING, 135 mm COLLIMATION LENS)

This approach may also be used to calibrate the O.M.A. with any other optical input pattern that does not extend beyond the edges of the "signal" or "light" half of the detector scan area.

The procedure is as follows.

(1) A standard PRESET number of accumulation cycles appropriate to the reference source must be selected.

(2) Perform a PRESET reference signal accumulation into the "A" memory (PRESET HOLD, A ACCUM).

(3) Turn off the reference source and perform an equal PRESET background accumulation (B ACCUM) into the "B" memory.

(4) Set the A-B DISPLAY SELECT pushbutton and use the Channel Summing Mode (Σ, see Subsection 3.3B) to sum all the channels in the reference signal peak.

(5) The resulting value is independent of minor errors in focus, optical alignment, image size, etc. Readjust the RAMP control if necessary (clockwise will increase the MAGNITUDE indication for a given input signal), and repeat steps (2) through (5) until the indicated net integrated peak area is at the correct reference value.

(6) Check the peak-to-peak voltage of the reference ramp at TP-6 on the INPUT card. This is nominally 10.0 V, but may be set between 8.0 V and 12.0 V pk-pk for this calibration.

Note that, although turning the RAMP control counterclockwise *appears* to increase the sensitivity of the instrument, this is actually limited by the signal-to-noise ratio of the system. Thus the primary effect of turning the RAMP setting to less than the normal 10 V is to reduce the usable dynamic range of a single scan. Increasing the RAMP setting increases dynamic range by trading off amplitude resolution.

8.9 FINE TUNING

Once reasonably good focus is obtained, the following suggestions may prove helpful in achieving the final optimum setting. Note that the appearance of the optimum focus on the CRT display will depend on the user's application. Also, since may of the adjustments interact or have similar-appearing effects, some care and patience or experience will be required to obtain optimum performance.

8.9A START OVER

If the adjustment procedure fails to produce a satisfactory focus or a level of performance that had been observed in the past, measure the voltages and signal levels and compare them with the initial settings in Subsection 8.5. If one or more of the detector electronics adjustments is set too far away from the initial or the ideal level, it may not be possible to achieve a correct setting by the interactive process discussed in Subsection 8.7. In this case, it is usually easier to return all adjustments to the initial settings and try again.

8.9B CENTERING THE IMAGE

Some of the focus and alignment adjustments will slightly alter the relationship between the input image and the detector scan pattern. In rotational alignment of the detector, this is caused by the location of the detector axis. The electronic focus adjustments cause a slight shift of the detector scan pattern relative to the input image. In either case, the light from an input slit image originally focused and centered on a single detector channel may be divided between two channels after the shift takes place.

During the initial rough focusing, the effect of an improvement in focus is readily visible even if the centering of

the input image on a single channel varies as the adjustment proceeds. But when the focus approaches the optimum setting, the slight shift in scan pattern can hide the optimum focus setting. Thus if the focus controls were simply peaked up, the slightly defocused adjustment would appear to be the correct setting.

Optimum performance is achieved by continuously re-centering the input signal over a single detector element during the fine tuning phase of the O.M.A. alignment. This is done as follows.

(1) Note the quality of the focus/alignment with a centered input.

(2) Make a slight focus/alignment adjustment.

(3) Recenter the input image by adjusting the input optics (e.g., Polychromator grating control) or by slight adjustment of the F. POSN trimmer on the O.M.A. FRAME SCAN card.

(4) Compare the CRT display with that in step (1) for possible improvement or reduction in performance (see Subsection 8.9C).

The input image is correctly centered over one detector element when *one* channel has a greater magnitude than the adjacent channels (if the image is 25 microns or narrower), and the adjacent channels appear in pairs of equal magnitude, on either side of the peak channel.

8.9C CROSSTALK AS FOCUS INDICATOR

When the focus adjustment approaches the optimum setting, the apparent crosstalk percentage becomes the best indicator of improvement as the adjacent proceeds.

The crosstalk takes a part of the signal from one detector channel element, and causes it to appear in the adjacent channels. Thus there will always be at least three channels in the CRT display peak, or two channels in each contrast transition in the case of a wide slit image. Once this condition is reached, further improvements in focus will not be reflected in a reduction in the width of the display peak. The optimum focus is reached by minimizing the apparent extra crosstalk caused by slight focus errors.

8.9D TOO-GOOD RESULTS

It is sometimes possible to achieve a setting that appears to completely eliminate crosstalk. This indicates some form of incorrect adjustment, usually a limit condition of incorrect BIAS setting. It is often characterized by poor sensitivity and/or a lack of the usual baseline curvature. See Subsections 8.6 and 8.9A.

SECTION IX
INTERFACING

9.1 GENERAL

The 1205A Optical Multichannel Analyzer (O.M.A.) has signal inputs and outputs available on its back panel to present measurement data in both analog and digital form and to allow remote programming of most O.M.A. functions. These signals may be divided into five groups:

(1) Analog output signals designed to display all 500 channels in graphic form on CRT displays and X-Y plotters.

(2) Parallel digital data outputs presenting a single channel of data, including a 12 bit, 3-digit Binary Coded Decimal (BCD) channel address (ADR12B1), and a 20 bit, 5-digit BCD word (DIG2ØB1) representing a magnitude. These outputs duplicate the information displayed on the front panel digital readout.

(3) Input/Output lines which both indicate and control most of the front panel pushbutton functions. As outputs, some of these lines define the significance of the magnitude on DIG2ØB1 by identifying the selected output function. As inputs, these lines parallel the pushbutton switches and can be used to remotely activate a function when the pushbutton is released.

(4) Remote program and timing signals.

(5) Control signals to allow automatic output of sequential channels to printers and incremental plotters, and to synchronize the digital output with various devices.

Also on the back panel are the signal/power connector for the 1205B, and spare connectors for option applications.

9.2 SIGNAL DESCRIPTION

9.2A ANALOG OUTPUTS (BNC CONNECTORS)

(1) CRT X: A sawtooth ramp of 32.8 ms period and approximately 1 V amplitude intended to drive the "X" or horizontal axis of oscilloscope (CRT) displays. This signal is normally synchronized with the O.M.A. memory cycle so that the ramp begins as channel zero appears on CRT Y, and returns to 0 volts at the end of the channel-499 display time. However, when the display is expanded with the front panel HORIZ EXPAND control, the timing of CRT X is altered to start twelve channel times prior to the channel selected by the cursor for digital display, and the ramp slope is determined by the setting of the HORIZ EXPAND control. To avoid overloading the scope in this mode, the ramp limits at approximately 3 V.

(2) CRT Y: A signal intended to drive the "Y" or vertical axis of a CRT display to provide a graph of 500 channels of input information. The amplitude of CRT Y scans sequentially through 500 channels in a 32.8 ms cycle, holding a value proportional to the three most significant digits (10^5, 10^4, 10^3) of each channel for a period of 64 μs. The SCALE FACTOR and VERT EXPAND front-panel controls allow the selection of lower order digits for display and an increase in the amplitude of CRT Y. When the display is expanded, CRT will limit at approximately 3 V to avoid overloading the scope input. In the LOG mode, this output is modified to provide a log-linear type display.

(3) CRT Z: A three-level signal of approximately ±1 V pk-pk amplitude intended to drive low-level "Z" (intensity) axis scope inputs. The three independently adjustable levels are as follows:

(a) A positive Z MARK level once per 32.8 ms cycle to identify the CRT trace over the channel selected by the cursor for digital readout.

(b) A negative Z BLANK level to blank the CRT trace during the retrace interval and during the settling time associated with each interchannel transition.

(c) A low positive Z LEVEL. The CRT intensity is normally set to just barely blank the beam with the O.M.A. turned off, preventing burned phosphors, and this level is set to provide the desired display brightness when the O.M.A. is turned on. This level is automatically increased in the HORIZ EXPAND mode to compensate for the reduced display time. This Z COMP is also independently adjustable.

(4) CRT Z HIGH: An intensity signal for use with scopes requiring a high-level (up to 25 V pk-pk) or inverted CRT Z signal. Internal controls allow adjustment of the amplitude and sense of CRT Z HIGH.

(5) VIDEO: An undigitized real-time signal output related to the REAL TIME CRT Y signal, and identified internally as VIDEOTPAN. The amplitude of this signal is adjustable. See Subsection 6.13E.

(6) PLOT X: Activating the PLOT/PRINT mode enables this slow positive ramp to drive the "X" axis of an X-Y plotter. Internally adjustable from one to 200 mV/s, the ramp stops after channel 499 has been plotted, and returns to zero when the PLOT/PRINT switch is released.

(7) PLOT Y: Activating the PLOT/PRINT mode enables this output. A sample and hold circuit samples the CRT Y signal for a single channel selected by the cursor and holds it on this output. The automatic

cursor advance in the PLOT/PRINT mode results in an X-Y plot of the portion of the O.M.A. data from the initial position of the cursor through channel 499, ending when the cursor returns to channel zero. Releasing the PLOT/PRINT switch returns the PLOT Y output to zero volts. The rate at which PLOT Y scans through the 500 O.M.A. channels (cursor advance rate) is set by the PLOT RATE switch, where a setting of "5" represents five 32.8 ms intervals per channel. A zero PLOT RATE setting allows the use of an incremental plotter, or in the REAL TIME mode, results in a plot of a single selected channel versus time.

(8) CURSOR: A 3 kΩ impedance output of a +3 V, 64 μs pulse which is high during the CRT Y output of the cursor-selected channel. It is provided for test purposes and as a channel marker for use with dual-trace scopes lacking an intensity input for CRT Z.

9.2B PARALLEL DATA OUTPUT LINES

(1) DIG2ØB1 (Digital Output #1-10 and 26-35)

This is the name of a twenty-signal buss with positive truth which will contain the five-digit Binary Coded Decimal (BCD) parallel output of the O.M.A. This number, corresponding to the MAGNITUDE portion of the front panel display, is identified by other signals and busses described below and can represent:

(a) The output of one channel of one memory.

(b) The difference (A-B) between one channel in the A memory and the same channel in the B memory.

(c) The result of a summation of several channels or differences such as (a) or (b) above.

(d) The digitized real-time value of the signal on the selected channel.

(e) The number of O.M.A. cycle times associated with the accumulation of the data in either memory. Total data accumulation time is this number times 32.8 ms.

(f) The difference (A-B) in the A and B memory accumulation times, in 32.8 ms O.M.A. frame times.

The twenty individual lines of this buss are named DIGØ1D1 (least significant bit) through DIG48D1 (MSB). The D1 indicates that the lines are digital and of positive truth. The two numbers ahead of the D1 indicate which bit of the word the line represents, where the first digit indicates the power of ten, and the second digit indicates the binary weight. Thus DIG24D1 is the 4 weighted bit of the 10^2 digit, and, when high, represents an increment of 400 in the value of the DIG2ØB1 buss. The entire 10^2 (100's) digit is composed of:

DIG21D1	(100)
DIG22D1	(200)
DIG24D1	(400)
DIG28D1	(800)

The buss name DIG2ØB1 tells us that there are 20 wires in the DIG buss. The B1 tells us that the name is for a buss with positive truth.

(2) DIGNEGD1 (Digital Output #11)

This is a signal with positive truth which is true (high) when the data on the DIG2ØB1 buss represents a negative number.

(3) SIGNORMDØ (Digital Output #36)

This signal is low except in the Σ (integration) or ACCUM CYCLES modes. It is included for use with P.A.R.C. modified Hewlett Packard #5055A printers to modify the normal "+" or "—" sign character to a "p" or "n" in the Σ mode.

(4) ADR12B1 (Digital Output #15-20 and 40-45)

This is the name of a 12 signal buss with positive truth which will contain the three-digit parallel BCD coded channel address for the data on the DIG2ØB1 buss. This number corresponds to the CHANNEL portion of the front panel display. The names of the individual signals are ADRØ1D1 through ADR28D1, coded in the same manner as the DIG2ØB1 buss.

9.2C INPUT/OUTPUT LINES

(1) DISPLAY SELECT

ASWDØ (Digital Output #14) DISPLAY SELECT pushbutton "A"
BSWDØ (Digital Output #13) DISPLAY SELECT pushbutton "B"
DIFFSWDØ (Digital Output #38) DISPLAY SELECT pushbutton "A-B"
REALSWDØ (Remote Program #47) DISPLAY SELECT pushbutton "REAL TIME"

The above four entries (ASWDØ, BSWDØ, DIFFSWDØ, and REALSWDØ) identify/control the corresponding front panel functions. As outputs they are negative truth, i.e., one of the four lines will be low to indicate that the corresponding pushbutton has been depressed. With ADR12B1, they indicate the source of the data on DIG2ØB1. Not more than one of the four should be active (low) at any one time.

(2) ACCUMCYSWDØ (Digital Output #21)

This negative truth line indicates/controls the ACCUM CYCLES front-panel function. When it is active (low), the information of ADR12B1 is meaningless, and

DIG2ØB1 represents an accumulation time in 32.8 ms O.M.A. frame times.

(3) INTSWDØ (Digital Output #12)

This negative truth line indicates/controls the Σ (Integrate) front-panel function. When it is active (low), DIG2ØB1 includes a scale factor of 10 or 100, and the channel number on ADR12B1 is that of the last channel included in the summation.

(4) INTX1ØDØ (Digital Output #37)

This negative truth line indicates/controls the scale factor in the Σ mode. If this line and INTSWDØ are both active (low), the DIG2ØB1 scale factor is 10. If this line is high while INTSWDØ is low, the scale factor is 100. If the rear-panel switch is set for X100, the X10 summation scale factor may be remotely selected by lowering this line *only when* INTSWDØ *is low.* When remotely programming X10 scale factor in this manner, both the X10 and the X100 front-panel lamps will be lit in the integrate X10 mode.

(5) LNZERODØ (Digital Output #49)

Line Number ZERO DØ is a low truth signal corresponding to the front panel ◄Ø► control. If held low for 100 ns or more it will reset the cursor to line number zero. This control overrides all other cursor controls.

(6) LOGSWDØ (Digital Output #24)

Indicates/controls the status of the front panel LOG display select switch. When active (low) the CRT and plotter displays will be in log-linear form.

(7) P/PSWDØ (Digital Output #46)

Indicates/controls the status of the front-panel (PLOT/PRINT SWITCH). Activating (lowering) this line starts the automatic plot/print operation with the O.M.A. channel selected by the cursor at that time.

(8) PREHOLDSWDØ (Remote Program #23)

Indicates/controls the status of the front-panel PRESET HOLD switch. When active (low), the preset hold counter will end an accumulation after the preset number of integration delay/frame scan cycles. When this line is high, the preset counter is reset.

(9) FSHOLDSWDØ (Remote Program #25)

Indicates/controls the status of the front-panel FULL SCALE HOLD switch. When this line is active (low), it will prevent further input accumulation if any channel in any memory selected for input has reached or passed a value of +98000.

(10) AACCUMSWDØ (Remote Program #50)

Indicates/controls the status of the A ACCUM input control switch.

BACCUMSWDØ (Remote Program #24)

Indicates/controls the status of the B ACCUM input control switch.

Each of the above two entries, when active (low), enables input accumulation into the corresponding memory. The actual accumulation starts and stops on a leading (rising) edge of a FRBLANKD1 (Subsection 9.2D-9) pulse. AACCUMSWDØ has no effect in the REAL TIME mode (REALSWDØ low).

(11) AMEMERSWDØ (Remote Program #48)

Indicates/controls the status of the A MEMORY ERASE switch.

BMEMERSWDØ (Remote Program #49)

Indicates/controls the status of the B MEMORY ERASE switch.

Each of the above two entries, if active (low) for 100 ns before and after the leading (rising) edge of FRBLANKD1 (Subsection 9.2D-9), will erase all 500 channels and the accumulate cycles counter of the corresponding memory, and zero the preset hold counter. Activating either line asynchronously for 33 ms or more will asure such a memory erasure.

Activating one of these lines while the corresponding AACCUMSWDØ or BACCUMSWDØ is active results in a mode similar to the REAL TIME mode in that memory, except that the previous memory contents are not saved. On the release (rise) of the memory erase line an accumulation ensues, the start time of which is the leading (rising) edge of the last FRBLANKD1 *prior* to the release of the memory erase.

9.2D REMOTE PROGRAM AND TIMING SIGNALS

(1) PGMPRE16B1 (16 inputs) (Remote Program #8, 16 through 22, 32, 33 and 41 through 46)

This is the name of the 16 wire, positive-truth, BCD-coded input buss that allows the remote programming of the PRESET switch function. The individual lines are named PGMPREØ1D1 through PGMPRE38D1, using the same coding scheme as the DIG2ØB1 buss. These lines are activated by PREPGMDØ.

(2) PREPGMDØ (Input) (Remote Program #5)

Lowering this line activates the PGMPRE16D1 buss. When this line is high, the front-panel PRESET thumbwheel switches set the accumulation interval in

the PRESET HOLD mode. When PREPGMDØ is low, the number coded on the PGMPRE16B1 buss replaces the front-panel setting.

(3) PGMDELØB1 (4 Inputs) (Remote Programs #6, 7, 30, and 31)

This is the name of the 4-wire, positive-truth, BCD-coded input buss that allows the remote programming of the DELAY switch function. The individual lines are named PGMDELØ1D1 through PGMDELØ8D1, using the same coding scheme as the DIG2ØB1 buss. These lines are activated by DELPGMDØ.

(4) DELPGMDØ (Input) (Remote Program #4)

Lowering this line activates the PGMDELØ4B1 buss. When high, the front-panel DELAY thumbwheel switch sets the integration delay. When DELPGMDØ is low, the number coded on the PGMDELØ4B1 buss replaces the front-panel setting.

(5) PGMLN12B1 (12 Inputs) (Remote Program #9 through 12, 14, 15, and 34 through 39)

This is the name of the 12-wire, positive-truth, BCD-coded input buss that allows the remote programming of the Line Number (Channel Number). The individual lines are named PGMLNØ1D1 through PGMLN28D1, using the same coding scheme as the DIG20B1 buss. These lines are activated by LNSTROBEDØ.

(6) LNSTROBEDØ (Input) (Remote Program #13)

Activating (lowering) this line strobes the three-digit number on the PGMLN12B1 buss into the cursor line number buffer. This line takes precedence over all other cursor controls except LNZERODØ (front-panel 0 switch). As long as LNSTROBEDØ is low, the data on the PGMLN12B1 buss will be forced into the cursor line number buffer and will not be affected by other cursor controls. If the line is raised, the programmed cursor line number will be retained until changed by a cursor control. For a proper strobe, this line must be low at least 50 ns and the PGMLN12B1 inputs must be stable for 40 ns before and after the rise of this line.

(7) LNADVCLKDØ (Input) (Digital Output #23)

Line Number Advance CLOCK DØ is a low-truth pulse input line for advancing the cursor line number counter by one. The trailing edge (low-to-high transition) of a low-going pulse will advance the line number. The pulse must be low for at least 50 ns.

(8) DELINHD1 (Output) (Remote Program #29)

This signal is low during any active input operation (REAL TIME mode, or an A and/or B memory accumulation without, or prior to, a full-scale or preset hold). It is useful as an indicator of the exact input interval in an asynchronous operation of the A ACCUM or B ACCUM modes, or of the exact ending time of a preset hold or full-scale hold accumulation (see Figures IV-5 and IV-6).

(9) FRBLANKD1 (Output) (Remote Program #28)

This FRAME BLANK pulse output consists of a 768 μs true (high) pulse once every 32.8 ms. This pulse corresponds to the twelve blank 64 μs channel times out of 512 that are the display retrace interval. All input and memory erase operations are clocked on and off by the leading (rising) edge of this pulse to insure that all channels are scanned an equal number of times. A flash event occurring during the first 600 μs of the FRBLANKD1 pulse will be scanned equally by all 500 channels (see Figures IV-5 and IV-6).

(10) FRRETRACEDØ (Output) (Remote Program #3)

This Frame RETRACE DØ pulse output consists of a 384 μs true (low) pulse once every 32.8 ms, at the beginning of FRBLANKD1. This pulse corresponds to the first six channel times of the twelve that make up FRBLANKD1, and is the retrace time of the vidicon. The ACCUM CYCLES output is transferred by the trailing (rising) edge of this pulse, and thus may be examined by fast output schemes without losing signal data channels.

(11) SDELAYDØ (Input) (Remote Program #40)

This signal, Stretch DELAY DØ, is intended for use by the Model 1207 extended delay option. When active (low) it disables the conventional DELAY mode (both the switch and PGMDELB1), and enables the direct control line DELBLANK2DØ. It also enables modification of the preset hold counter by the PRECLOCK2DØ input.

(12) DELBLANK2DØ (Input) (Remote Program #27)

When enabled by SDELAYDØ, this Delay BLANK #2 input replaces the conventional integration delay capability. When enabled and active (low), it prevents the scan/erasure of the vidicon by blanking the vidicon beam during an accumulation. It also inhibits quantization noise by disabling the 1205A input circuitry.

(13) PRECLOCK2DØ (Input) (Remote Program #2)

This input, PRESET hold counter CLOCK #2, allows the modification of the preset hold mode by modifying the clock input to the preset hold counter. When PRECLOCK2DØ is enabled by SDELAYDØ, the preset hold counter will:

(a) Not count at all when PRECLOCK2DØ is low.

(b) Increment on the leading (rising) edge of FRBLANKD1 during an accumulation when PRECLOCK2DØ is high. Preset hold then oper-

ates on the number of 32.8 ms frame times in the accumulation.

(c) Count negative-going (high-to-low) transitions of PRECLOCK2DØ at rates up to 5 MHz when FRBLANKD1 is low during an accumulation. Preset hold then operates asynchronously when the count reaches the selected number.

(14) +5BIAS1 (Output) (Digital Output #25)
+5BIAS2 (Output) (Remote Program #1)

Each of the above outputs is a 200 ohm resistor to +5 V, to provide a source of TTL "1" for programming purposes.

9.2E OUTPUT CONTROL SIGNALS

(1) General

The 1205A has two basic sets of output control signals. One, consisting of PRINTCMDDØ and PRINTINHDØ, is intended for use in the O.M.A.'s automatic I/O mode which is of particular value for plotting or printing the contents of a memory. When in this mode there is an automatic advance of line number, either at a fixed rate selected by the PLOT RATE switch (which varies between 32.8 ms/line) or in an asynchronous mode (with the rate switch at "0") using the Print Inhibit and Command Lines.

The second, DATAREQDØ and DATAREADYD1, is useful for data transfers to computers.

The available data rates are the O.M.A. line scan rate of 500 sequential channels in 32.8 ms (64 μs channel), or some multiple of the frame scan rate, which is one readout in 32.8 ms.

(2) PRINTCMDDØ (Output) (Digital Output #48)

The PRINT COMMAND DØ line will go low when the 1205A is in the PLOT/PRINT mode to indicate that a datum is available on the parallel data lines to be printed or plotted (or used by any other similar device). This line will stay low until a PRINTINHDØ response is received.

(3) PRINTINHDØ (Input) (Digital Output #47)

This is a command line, PRINT INHIBIT, from the printer (etc.) to the O.M.A. which is lowered in response to a print command. Its effect is to clear PRINTCMDDØ when PRINTINHDØ goes low, and if the PLOT RATE switch is set at zero, to advance the line number when PRINTINHDØ rises on completion of the print cycle. If the PLOT RATE switch is not at zero, the line number is advanced at the selected rate which must be slower than the printer's maximum speed. In either case, the process is terminated after the last channel (#499) is read.

(4) DATAREQDØ (Input) (Digital Output #22)

DATAREQUESTDØ is a command line to the 1205 useful for data transfers to computers. When this line is high, DATA READY will be cleared.

When low (true), Data Ready will set when new data is available.

(5) DATAREADYD1 (Output) (Digital Output #39)

This is a line that goes high when a requested data word becomes available in the output register and the Data Request is low. The combination of both Data Ready and Data Request being true will prevent the change of data.

TTL DIGITAL OUTPUT				TTL REMOTE PROGRAM			
DIGØ1 D1	1	26	DIGØ4 D1	+5BIAS2	1	26	GROUND
DIGØ2 D1	2	27	DIGØ8 D1	PRECLOCK2 DØ	2	27	DELBLANK2 DØ
DIG11 D1	3	28	DIG14 D1	FRRETRACE DØ	3	28	FRBLANK D1
DIG12 D1	4	29	DIG18 D1	DELPGM DØ	4	29	DELINH D1
DIG21 D1	5	30	DIG24 D1	PREPGM DØ	5	30	PGMDELØ8 D1
DIG22 D1	6	31	DIG28 D1	PGMDELØ4 D1	6	31	PGMDELØ2 D1
DIG31 D1	7	32	DIG34 D1	PGMDELØ1 D1	7	32	PGMPREØ8 D1
DIG32 D1	8	33	DIG38 D1	PGMPREØ4 D1	8	33	PGMPREØ2 D1
DIG41 D1	9	34	DIG44 D1	PGMLNØ8 D1	9	34	PGMLNØ4 D1
DIG42 D1	10	35	DIG48 D1	PGMLNØ1 D1	10	35	PGMLNØ2 D1
DIGNEG D1	11	36	SIGNNORM DØ	PGMLN18 D1	11	36	PGMLN14 D1
INTSW DØ	12	37	INTX10SW DØ	PGMLN11 D1	12	37	PGMLN12 D1
BSW DØ	13	38	DIFFSW DØ	LNSTROBE DØ	13	38	PGMLN28 D1
ASW DØ	14	39	DATAREADY D1	PGMLN22 D1	14	39	PGMLN24 D1
ADRØ1 D1	15	40	ADRØ4 D1	PGMLN21 D1	15	40	SDELAY DØ
ADRØ2 D1	16	41	ADRØ8 D1	PGMPRE18 D1	16	41	PGMPRE14 D1
ADR11 D1	17	42	ADR14 D1	PGMPRE12 D1	17	42	PGMPRE11 D1
ADR12 D1	18	43	ADR18 D1	PGMPRE31 D1	18	43	PGMPRE32 D1
ADR21 D1	19	44	ADR24 D1	PGMPRE34 D1	19	44	PGMPRE38 D1
ADR22 D1	20	45	ADR28 D1	PGMPRE21 D1	20	45	PGMPRE22 D1
ACCUMCYSW DØ	21	46	P/PSW DØ	PGMPRE24 D1	21	46	PGMPRE28 D1
DATAREQ DØ	22	47	PRINTINH DØ	PGMPREØ1 D1	22	47	REALSW DØ
LNADVCLK DØ	23	48	PRINTCMD DØ	PREHOLDSW DØ	23	48	AMEMERSW DØ
LOGSW DØ	24	49	LNZERO DØ	BACCUMSW DØ	24	49	BMEMERSW DØ
+5BIAS1	25	50	GROUND	FSHOLDSW DØ	25	50	AACCUMSW DØ

Table IX-1. MODEL 1205A OMA INTERFACE INFORMATION

9.3 ELECTRICAL CONSIDERATIONS

9.3A SIGNAL LEVELS

(1) Outputs

Output signals may be used to drive one (and not more than one) standard TTL load (i.e., they will sink 1.6 mA to less than 0.4 V and will drive 50 μA at not less than 2.6 V).

(2) Inputs

The 32 individual lines in the PGMDELØ4B1, PGMPRE16B1, and PGMLN12B1 busses each represent one standard TTL load ("1" = >+2.6 V @ 50 μA, "Ø" = <0.8 V @ −1.6 mA). All other input lines require drivers capable of driving 10 standard TTL loads.

(3) Input/Output Lines (listed in Subsection 9.2C)

These lines are shorted to ground when the corresponding front-panel switch is depressed, and should not be driven with "totem pole" (e.g., 7400, etc.) drivers. Each of these lines will drive at least one standard TTL load, and may be driven by a single pole switch to ground or by an otherwise uncommitted open collector TTL gate (7401 or equivalent).

9.3B TERMINATION

The signals on list 1A and 1B must be on twisted pairs with a typical impedance of 120 Ω. The signals on list 1A are to be driven by the circuit shown in Figure IX-1. Signals on list 1B should be terminated as shown in Figure IX-2. All wires are to be less than 6 feet in length from the 1205A connector to the terminating circuit.

LIST 1A	LIST 1B
LNSTROBEDØ	DELINHD1
LNZERODØ	FRBLANKD1
LNADVCLKDØ	FRRETRACEDØ
DATAREQDØ	DATAREADYD1
PRINTINHDØ	PRINTCMDDØ
DELBLANK2DØ	
PRECLOCK2DØ	

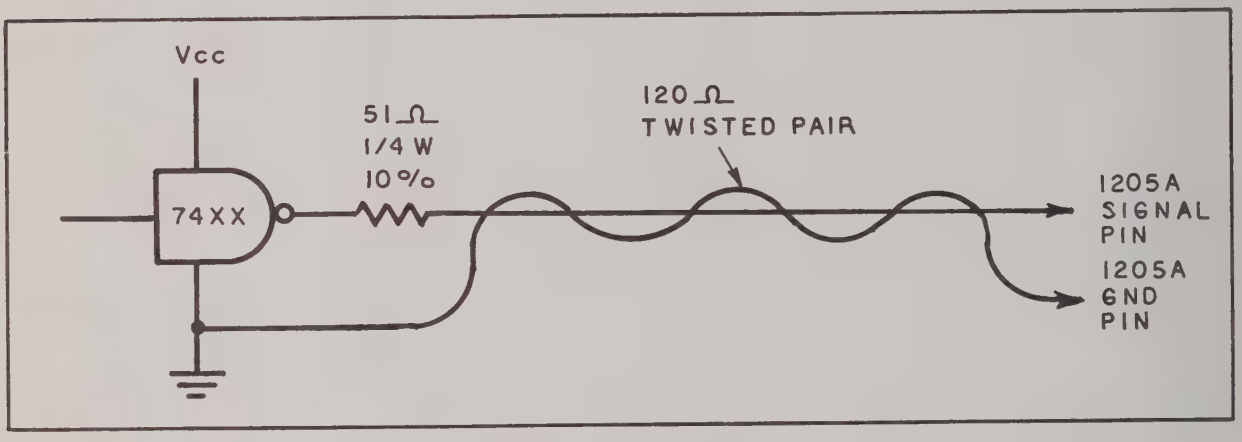


Figure IX-1. DRIVING CIRCUIT

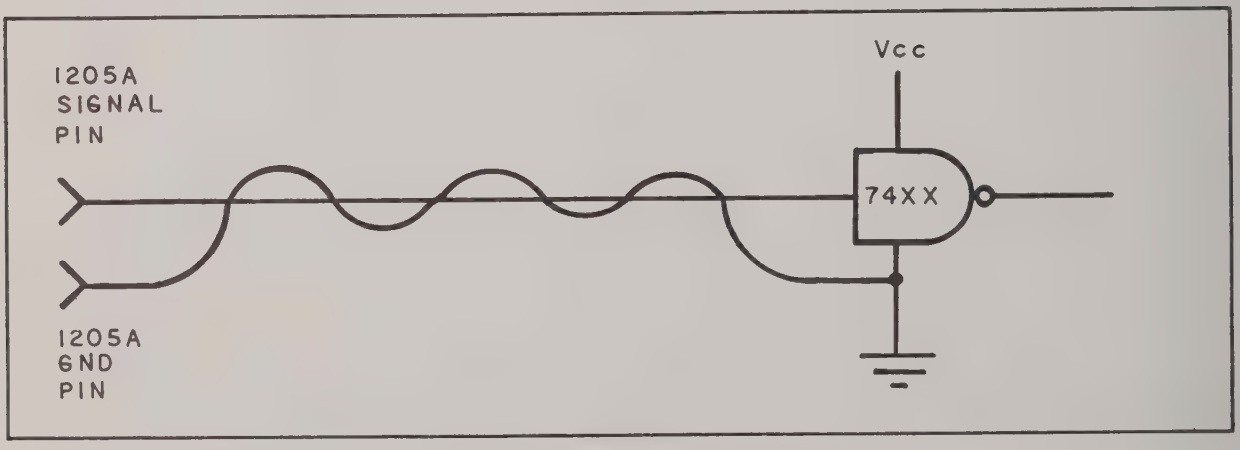


Figure IX-2. TERMINATING CIRCUIT

SECTION X
CIRCUIT DESCRIPTION

10.1 GENERAL

The 1205B DETECTOR ASSEMBLY has an input array of 500 parallel lines which are sensitive to a broad range of optical wavelengths. On the target of the vidicon, the light is converted to a charge and stored for readout. To read the contents of a channel, the vidicon's electron beam is scanned up and down a line. The beam current recharges the target and causes an output current equivalent to the accumulated light input. The target current is amplified and sent to the input processor in the 1205A.

The INPUT CARD of the 1205A integrates the signal from the vidicon and produces a voltage equivalent to the difference between the light accumulated on the top half of each line and the light accumulated on the bottom half of each line of the vidicon target. This process subtracts out the dark current in the target. The voltage which results is compared with a ramp, yielding a voltage to pulse width conversion.

The pulse from the INPUT CARD is used to gate a 16 MHz clock which is directed to one of the five-digit BCD counters on the MEMORY CARDS. On each MEMORY CARD there is a 512 word shift-register memory. For each line scanned by the vidicon, there is a word in the shift register associated with that line. The data for a particular line is added to the contents of the shift register by shifting the data into the counters, counting the pulses resulting from the voltage to pulse conversion, and loading the data back into the shift register.

The contents of each of the 500 memory channels represent the sum of many analog-to-digital conversions of the signal from each of the 500 lines on the vidicon.

The accumulated data is gated out of the counters on each memory and passed through the arithmetic section. From the arithmetic unit the data may go to the digital-to-analog converter for use by the X-Y display, or to the front panel as digits. At the digital display, the data from only one channel at a time is of interest. The desired channel is selected by a three-digit up/down counter which is read out on the front panel. This number, the cursor line number, is set by the front-panel cursor controls. It is compared with the contents of a second counter, the line-number counter, which is synchronized to the rotation of the shift register and also to the vidicon sweep. A "compare" between the two counters indicates that the data from the arithmetic unit is from the desired channel, that is, the cursor number equals the line number.

For convenience in accumulating data, there is a register which counts input cycles. This number is compared with the front panel preset switches and, if the preset hold mode has been selected, stops an accumulation on a "compare".

A machine cycle is a complete scan time. This is also the time for the shift register to make one complete revolution. An accumulation cycle is the time between successive readouts of the same line on the vidicon. An accumulation cycle may be any integral number of machine cycles. Time between readouts of the vidicon is measured in delay cycles, in which the vidicon beam is blanked and accumulations to memory are inhibited. Delay cycles are counted by the delay-cycle counter on the PRESET CARD, and the number of delay cycles is set by the front-panel DELAY switch.

The machine cycle is divided into two major times: an active time when the vidicon beam is normally sweeping the 500 lines, and a blanking time during which the vidicon beam is blanked and retraced. The machine cycle may also be broken into 512 line times, corresponding to the 512 words in the memory. The active time takes 500 line times; the blanking interval takes twelve. The line time is broken into smaller time segments by the timing card to control the various parts of the 1205A. The timing for a machine cycle time (512 line times) is generated on the CURSOR CARD, and the longer cycles (delay and preset) are timed by the PRESET CARD.

10.2 INPUT CARD

As indicated by the System Block Diagram (Figure X-1), the function of the INPUT card is to accept the detector preamplifier output from each of the 500 channels and convert it into a TTL digital pulse whose width is related to the signal light intensity from that channel. This pulse, TGATED1, goes to the TIMING card where it gates a burst of 16 MHz clock pulses, COUNTCLOCKD1. In the REAL TIME or ACCUMULATE modes, this burst of clock pulses is counted by a memory counter to provide a BCD digital value for the signal input. The input card performs its function during each 64 μs channel input time. The INPUT card also includes the TEST mode input signal generator and the power-on reset function.

10.2A BLOCK DIAGRAM

The INPUT card operation may be divided into two major functions: analog subtraction and analog-to-digital (A-D) conversion. During each 64 μs interval, the output from one channel element is undergoing A-D conversion while the signal from the next channel is being scanned at the vidicon target and processed by the scan-beam chopping circuitry.

The analog subtraction circuitry is controlled by Q6D1 (see Input Card schematic) to form a synchronous detector for light on the "signal" half of the detector target. The "dark" half of each detector channel element (scan line) is scanned during the first 32 μs of the cycle while Q6D1 is low. While Q6D1 is low, a positive signal from the detector preamplifier will cause the integrator output to go negative. As the "signal" half of the target is scanned in the next 32 μs, Q6D1 is high, so that a positive signal causes the integrator

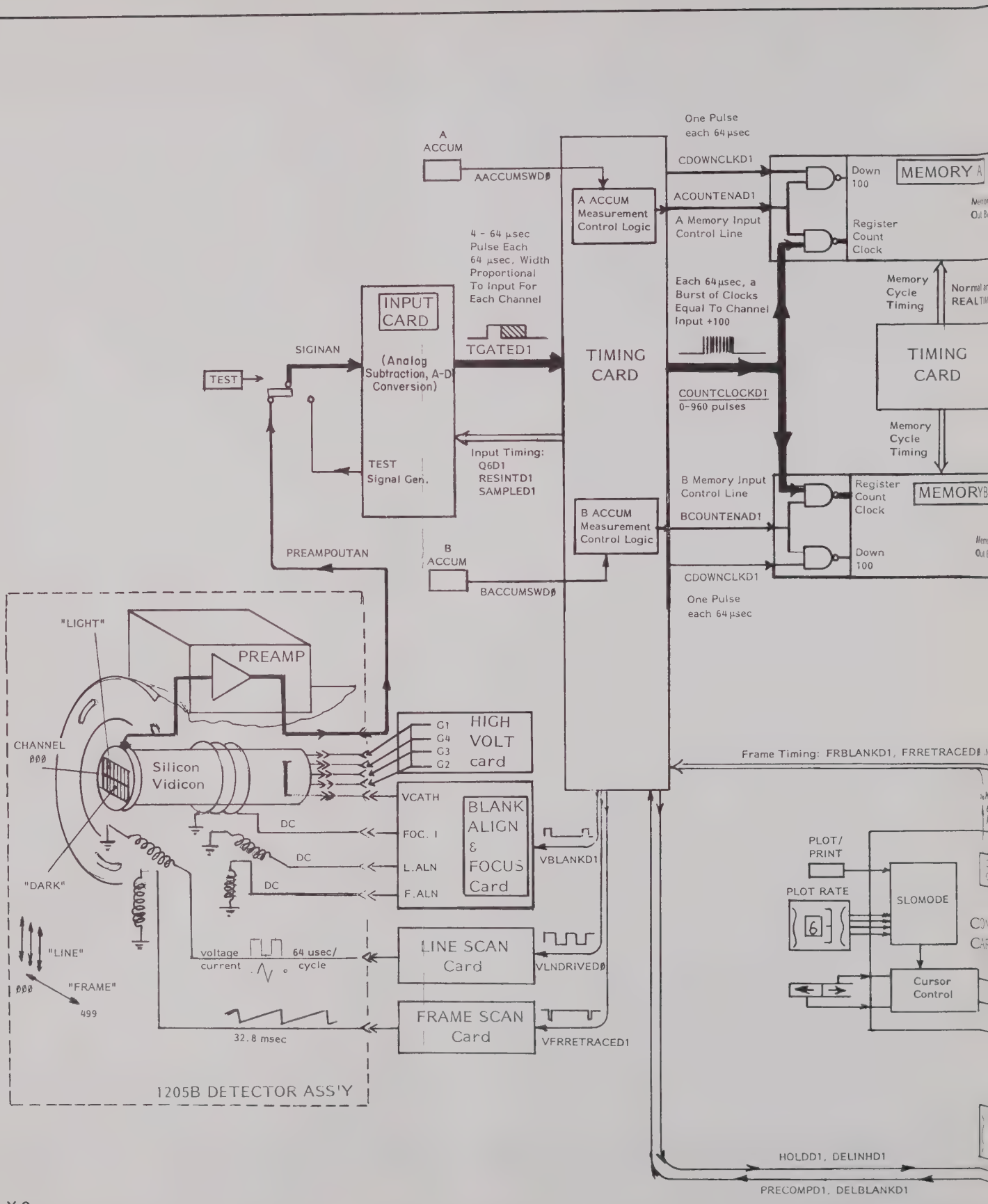
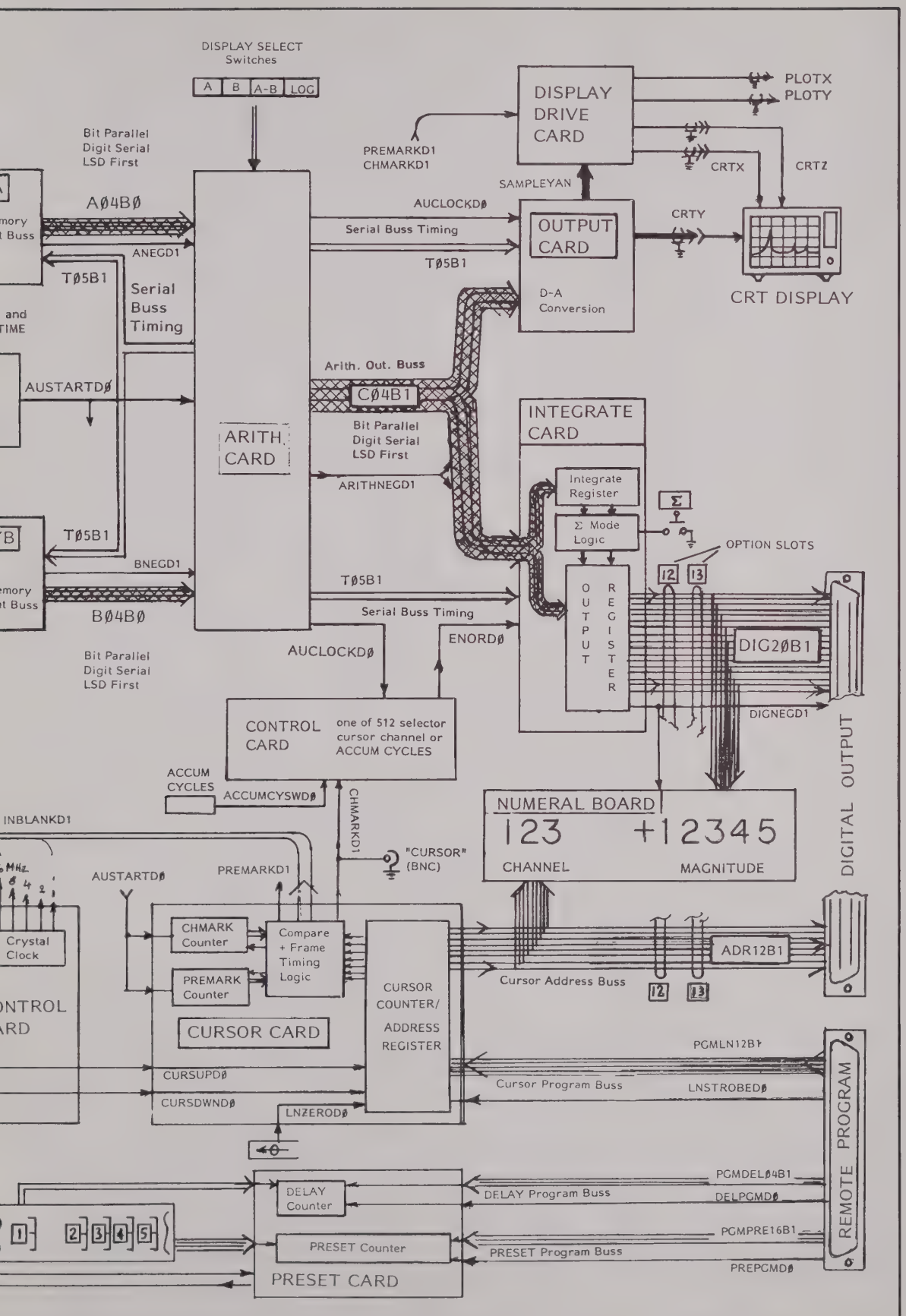


Figure X-1. SYSTEM BLO


DISPLAY SELECT Switches
A
B
A-B
LOG
DISPLAY DRIVE CARD
PLOTX
PLOTY
CRTX
CRTZ
CRTY
CRT DISPLAY
PREMARKD1
CHMARKD1
SAMPLEYAN
AUCLOCKDØ
Serial Buss Timing
TØ5B1
OUTPUT CARD
D-A Conversion
Bit Parallel Digit Serial LSD First
AØ4BØ
ANEGD1
Serial Buss Timing
AUSTARTDØ
Arith. Out. Buss
CØ4B1
ARITH CARD
Bit Parallel Digit Serial LSD First
ARITHNEGD1
INTEGRATE CARD
Integrate Register
Σ Mode Logic
OPTION SLOTS
OUTPUT REGISTER
DIG2ØB1
DIGNEGD1
BNEGD1
BØ4BØ
Serial Buss Timing
ENORDØ
AUCLOCKDØ
CONTROL CARD
one of 512 selector cursor channel or ACCUM CYCLES
ACCUM CYCLES
ACCUMCYSWDØ
CHMARKD1
NUMERAL BOARD
123
+12345
CHANNEL
MAGNITUDE
DIGITAL OUTPUT
INBLANKD1
"CURSOR" (BNC)
AUSTARTDØ
PREMARKD1
Crystal Clock
CHMARK Counter
PREMARK Counter
Compare + Frame Timing Logic
CURSOR CARD
CURSOR COUNTER/ ADDRESS REGISTER
ADR12B1
Cursor Address Buss
PGMLN12B1
Cursor Program Buss
LNSTROBEDØ
CURSUPDØ
CURSDWNDØ
LNZERODØ
REMOTE PROGRAM
DELAY Counter
DELAY Program Buss
PGMDELØ4B1
DELPGMDØ
PRESET Counter
PRESET Program Buss
PGMPRE16B1
PREPGMDØ
PRESET CARD

CK DIAGRAM

output to go positive. DC signals such as dark current and preamplifier offset integrate to zero over the full 64 μs cycle, so the integrator output at the end of the Q6D1 cycle represents the net light accumulated on the "signal" half of the detector element since the last scan. This level is transferred into the sample-hold circuit by SAMPLED1, which also resets the A-D converter.

The signal at the sample-hold circuit is compared with a reference ramp by a circuit whose output is true (TTL high) whenever the sample hold output is more positive than the ramp voltage. Thus the comparator output TGATED1 is a positive pulse whose width varies from 4 to 64 μs in proportion to the input signal amplitude.

The signal at the sample-hold point is buffered and presented at the rear-panel VIDEO connector. It is similar to the REAL TIME CRT output, with a negative offset. A gain trimmer is provided.

The TEST input signal generator circuit provides a signal synchronized with Q6D1 and CHMARKD1, which will be recognized by the scan beam chopping circuits as a positive signal input. The TEST mode switch (front panel) substitutes this signal for the detector preamplifier output.

The power-on reset circuit sets the cursor and both memories to zero when the O.M.A. system power is first turned on.

10.2B ANALOG SUBTRACTION

The Analog Subtraction circuitry consists of the inverting amplifier IC-3, integrating amplifier IC-4, and the two TTL-controlled FET switches of IC-1. Both amplifiers are N5556V operational amplifiers.

One complete analog subtraction cycle takes place during each 64 μs cycle of the timing signal Q6D1. Q6D1 may be observed at testpoint TP7, at the top left corner of the card. The cycle begins as Q6D1 goes low, and RESINTD1 goes high. The detector is just beginning to scan the "dark" half of a channel element. (See timing diagrams: Figures XII-2 and XII-3.) RESINTD1 is high during the first 4 μs of the cycle, causing inverter 2a to go low, closing FET switch 1a. This discharges capacitor C1, resetting the integrator. Since the integrator is held in the reset condition for the first 4 μs of the input cycle, this portion of the signal from the "dark" half of the detector element is ignored.

At the end of the reset interval, RESINTD1 goes low, FET switch 1a opens, and the current appearing at the summing junction (IC-4, pin 2) is integrated. Since Q6D1 is low at this time, FET switch 1b is closed, providing two signal paths to the integrator. An input signal, for example +1 V at TP1, passes through the unity-gain inverter composed of IC-3, R4, and R2. The −1 V at TP2 will cause a 0.2 mA of current to flow out of the summing junction via R5.

However, while Q6D1 is low, the non-inverted signal at TP1 is applied directly to the summing junction via R11, R12, and FET switch IC-1b. The SYMMETRY trimmer R11 is normally adjusted so that the current in this path is exactly twice that in R5, i.e., R11 + R12 = 2.55 kΩ. In the +1 V example, 0.4 mA will flow into the summing junction via this path. The net current at the summing junction will thus be 0.2 mA *into* the junction, which will cause the integrator output (TP3) to go negative. After 28 μs the +1 V input will yield −1.87 V at TP3.

This input mode continues for 28 μs until the end of the first half of the 64 μs Q6D1 cycle. At this point (the end of microsecond #31 in Figure XII-4), the detector scan moves from the "dark" half of the target and begins to scan the "signal" half of the detector element, and Q6D1 goes high.

When Q6D1 goes high, FET switch 1b will open. A +1 V signal at the input will now produce 0.2 mA *out* of the summing junction, and will cause the integrator output to go positive.

Eight microseconds before the end of the Q6D1 cycle (microsecond #56 in Figure XII-4), SAMPLED1 goes high. This is inverted by IC-2e, closing FET switch 5b, connecting the sample-hold capacitor C4 to the integrator output. SAMPLED1 is high for 4 μs, allowing C4 time to charge to the integrator output voltage. Since C4 is tracking the integrator output when SAMPLED1 goes low, and opens FET switch 5b, the capacitor holds the integrator output value at the instant the switch opens. This is the end of microsecond #59, or at the end of 28 μs of the "signal" half of the cycle. The last 4 μs of the "signal" half of the cycle are not used, to balance the 4 μs of the "dark" area lost during the RESINTD1 interval at the beginning of the cycle.

If the +1 V input signal of the example were due to dark current or preamplifier offset, it would be constant over the entire 64 μs cycle. The integrator will go negative for 28 μs during the "dark" half cycle, and positive for 28 μs during the "signal" half cycle, resulting in zero net output at the sample-hold point. Thus dark current and amplifier offset, and particularly the large temperature coefficient of dark current, are eliminated. Light on the "signal" half of the target detector element will cause the preamplifier output to be more positive during the "signal" half cycle than during the "dark" half cycle, resulting in a net positive effect at the end of the integrator cycle.

The BIAS trimmer is connected to a reference voltage (VR2 and VR3) to provide an adjustable bias current to the integrator summing junction via R13. This bias current is adjusted to set the zero-signal integrator output to the "zero" level required by the A-D converter. This level is normally about −4 V (or −1 V in the "400" mode).

The analog subtraction circuitry will provide an output that is a linear function of input "signal" light independent of dark current as long as the combined effect of signal, dark current, and bias current does not cause the integrator to reach a limit at ±13 V at any time during the Q6D1 cycle.

10.2C ANALOG-TO-DIGITAL (A-D) CONVERSION

The A-D Conversion for each channel, channel 250 for example, takes place during the 64 μs interval from the beginning of a SAMPLED1 pulse to the beginning of the next SAMPLED1 pulse (microsecond #56 through micro-

second #55, Figure XII-4), as the following channel (#251) is processed by the analog subtraction circuitry.

At the end of the SAMPLED1 pulse, the analog subtraction output appears as a stable voltage on the sample-hold capacitor C4 (TP4). This voltage is compared with a reference ramp generated by IC-7, C6, and FET switch 5a. While SAMPLED1 is high, FET switch 5a is closed, which resets the ramp generator to the reference voltage set by VR2. VR1, VR2, and VR3 are 5.1 V, 5% zeners, so the ramp generator resets to a stable value in the range −5.1 V ±0.3 V. IC-7 is a high-slew-rate operational amplifier, allowing the ramp to be reset in the first microsecond of SAMPLED1.

At some point during this interval, the ramp output (TP6) will become more negative than the signal sample at TP4. This causes the output of the comparator, IC-6, to transition from about −13 V to +13 V, the output limits. R14, CR1, and CR2 clamp the TGATED1 output to TTL levels, and the very high slew rate of IC-6 results in 50 ns TTL rise and fall times for TGATED1.

When SAMPLED1 goes low at the end of microsecond #59 (Figure XII-4), FET switches 5a and 5b open, and the ramp generator begins to integrate a constant current set by VR1, R24, and the RAMP trimmer R25. This trimmer is adjusted for a 6 μs/volt linear ramp rate during the remaining 60 μs of the cycle. When the ramp voltage at TP6 becomes more positive than the signal sample at TP4, the TGATED1 comparator output goes low. Thus the TGATED1 high pulse width consists of the 4 μs SAMPLED1 interval plus an interval that is proportional to the signal level at TP4, measured relative to the 5.1 V ramp reset level (see Figure XII-2).

The non-SAMPLED1 portion of TGATED1 (i.e., TGATED1 − SAMPLED1) is used on the TIMING card to gate a burst of 16 MHz clocks (COUNTCLOCKD1), which are counted by the memory counters when in the ACCUM or REAL TIME modes. These counters see zero-to-960 clocks per channel time, as the TGATED1 pulse varies from 4 to 64 μs in response to input signal.

Note that the TGATED1 pulse displays leading-edge jitter related to the previous and current signal-sample levels, and to the ramp reset time. This jitter is eliminated in later circuitry. However, in order to view the TGATED1 pulse, it is necessary to trigger the scope on a stable signal such as Q6D1 or SAMPLED1. Triggering on the CURSOR output (CHMARKD1) will display the TGATED1 pulse for a selected channel, allowing the signal level to be compared with the TGATED1 pulse width.

10.2D "NEGATIVE" SIGNAL

To accommodate negative signals, the memory counters are offset by −100 counts by a CDOWNCLKD1 pulse during the SAMPLED1 interval. The input card BIAS trimmer is then adjusted so that a zero-signal input produces exactly 100 pulses at COUNTCLOCKD1 (i.e., approximately −4.1 V @ TP4 or TGATED1 = 10.25 μs). The net effect at the end of the conversion will be a REAL TIME mode MAGNITUDE reading of zero. However, if the noise component of the dark current and stray light causes the detector "dark" output to exceed the "signal" output, the analog subtraction output may go more negative without exceeding the A-D conversion range. If, for example, TP4 drops to −4.5 V, TGATED1 will be 7.75 μs, or 60 COUNTCLOCKD1 pulses added to the −100 CDOWNCLKD1 offset. The resulting REAL TIME MAGNITUDE reading would be −40. The 960 counts of A-D conversion range therefore provide a −100 to +860 signal range.

The "400 mode" is provided to accommodate experiments in which the "dark" level is large compared to the signal input. In this mode a switch on the TIMING card selects a burst of four CDOWNCLKD1 pulses during SAMPLED1 time, offsetting the memory counter by −400. The input card BIAS trimmer is then readjusted for a zero-input REAL TIME MAGNITUDE reading of +00000, which is exactly 400 COUNTCLOCKD1 pulses, or approximately −1.1 V at TP4 and 29 μs at TGATED1. The input signal range is now −400 to +560 counts.

10.2E INPUT SIGNAL LIMIT

In normal operation, the maximum input signal is limited by the A-D conversion range. This allows the approaching limit condition to be detected digitally on the TIMING card while the instrument is still operating in the linear region. The usable signal maximum is also affected by the fact that the arithmetic cycle occupies a part of the 64 μs conversion time. In the REAL TIME mode, the A-D conversion must be completed in time to transfer the resulting data to the output logic before the end of the 64 μs channel time.

The "error LED" is therefore lit to indicate an input limit condition whenever the TGATED1 pulse for any channel is still high at AUSTARTDØ time. This occurs at 832 COUNTCLOCKD1 pulses or a front panel MAGNITUDE of +732. (MAGNITUDE = +432 in the "400 mode".) This is at the beginning of microsecond #48 in Figure XII-4. The limit detecting logic is actually located on the TIMING card.

Since the actual data transfer takes place during the second half of the arithmetic cycle, the REAL TIME output will continue to be correct up to MAGNITUDE = +783 (883 COUNTCLOCKD1 pulses). This provides a 7% linear overrange in the REAL TIME MODE.

ALL COUNTCLOCKD1 pulses will be properly counted into memory. Thus the A ACCUM and B ACCUM modes allow up to 959 counts (MAGNITUDE = +859) per channel per input cycle, since the extra counts are stored in memory for later display. The numeric and CRT display outputs may be incorrect during the accumulation process when the error LED is lit, but the correct memory contents will be correctly displayed once the input overload ends or the accumulation process is completed. This represents 17% linear overrange in the ACCUMULATE modes.

10.2F VIDEO

The input signal, after analog subtraction but before A-D conversion (i.e., the TP4 signal), is buffered and presented at the rear panel VIDEO connector. This signal, identified

as VIDEOTPAN, may be set to any convenient amplitude by adjusting the VIDEO trimmer on the INPUT card. It is buffered by the Darlington emitter follower pair Q1-Q2.

Since the INPUT card is active at all times, the VIDEO output allows the input signal to be examined while not in an ACCUM or REAL TIME mode, or when use of the REAL TIME mode is prevented by an A ACCUM operation.

10.2G TEST INPUT SIGNAL GENERATOR

The TEST signal generator consists of Q3, Q4, and the associated components. The circuit generates an adjustable amplitude, synchronous signal of the sort required to cause a signal output from the analog subtraction circuits (see waveform Figure XII-2). When the front-panel TEST switch is depressed, the TEST signal replaces the detector preamplifier output as the signal source for the INPUT card. Pressing the TEST switch also activates the TEST status indicator LED.

Q6D1 is low during the "dark" half of the input cycle. This causes a high level at the output of inverter 2f which turns on transistor Q4. When Q4 is saturated, both ends of the TEST trimmer (R15) are grounded, and the TESTOUTA+ signal is zero. During the "signal" half cycle, Q6D1 is high and Q4 is cut off, allowing TESTOUTA+ to go positive. As explained in Subsection 10.2B, a positive input during the "signal" half cycle will have the same effect on the O.M.A. console as "signal" light on the detector.

This signal amplitude is determined by the setting of the TEST TRIMMER (R15) and by the state of transistor Q3. CHMARKD1 is low during most of the 512 channel input cycles, which causes a high level at the output of inverter 2b and saturates Q3. The maximum TESTOUTA+ voltage at the CW end of the TEST trimmer will be about +2 V during the "signal" half cycle.

CHMARKD1 is high during the 64 μs output time of the cursor-selected channel. This cuts off Q3, increasing the maximum "signal" TESTOUTA+ to about +3.5 V. Because of the difference in the input and output 64 μs channel times, if the cursor is set at CHANNEL = 250, the extra TESTOUTA+ signal occurs during the last 12 μs of the channel 251 input cycle, and the first 16 μs of the "signal" half of the channel 252 input cycle. This causes the characteristic 2 to 3.5 V step in the two channels following the cursor marker.

10.2H POWER-ON RESET

The circuit composed of R28, C19, Q5, Q6, inverter 2C, and the four gates of IC-8 generates a power-on reset pulse. When the 1205A is first turned on, capacitor C19 will be discharged. This will cause the output of the series emitter followers Q5 and Q6 to go low. The output of inverter 2C will be high, and the four open-collector outputs of gates 8A, B, C, and D will be low. Holding the LNZERODØ, AMEMERSWDØ, and BMEMERSWDØ lines low has the same effect as pressing the front-panel memory erase and cursor zero switches, i.e., the cursor and all memory channels are reset to zero. After about two seconds, C19 will be charged to a high enough level to turn off the reset pulses. SYSRESETDØ is a spare reset line for use by options.

10.3 MEMORY CARDS

The 1205 has two identical MEMORY CARDS. Each contains 512 words of 5 BCD digits plus sign bit. When not being manipulated, the data is stored in 21 one-bit by 512-bit MOS dynamic shift registers.

These shift registers have parallel clocks, SHIFTINDØ and SHIFTOUTDØ, which respectively shift a 21 bit word from the BCD counting register into the shift registers or shift a new word out of the shift registers onto the counting registers' parallel input lines.

The memories have four modes of operation: (1) Erase, (2) Accumulate, (3) Store, and (4) Real Time. Because the MOS memories are dynamic (i.e., they must be running to retain data), the shift clocks are present in all modes. The clocks occur at the line rate (i.e., every 64 μs) to maintain synchronism between the vidicon scan and the memories. Each memory makes a complete 512 word "rotation" every frame time. The shift pulses both occur during the 4 μs SAMPLE PULSE.

With the rise of SAMPLED1, SHIFTINDØ goes true (low), and stays true for 1 μs. One 1 μs after SHIFTINDØ goes not true (high), SHIFTOUTDØ goes true (low) for 1 μs. The two clock pulses are buffered, level shifted, and shortened by IC-28 and MOS clock driver IC-27. The output pulses are negative going, approximately 400 ns long, timed from the fall of the input pulse, and switch from +5 V to −12 V. The timing of these pulses is the same for all modes of operation.

In the erase mode, a 1 μs low-going pulse is applied to the A/BMEMERASEDØ line immediately after the rise (end) of SHIFTOUTDØ. This pulse resets the five BCD counters (IC's 22, 23, 24, 25, 26) to zero and in the absence of a count enable (A/BCOUNTENAD1), this zero data will be shifted back into the shift register on the next shift-in clock. The reset pulse also resets the sign flip-flop, IC-36, to the state which signifies a plus.

To clear the entire memory, this process must be repeated 512 times, that is, for one complete machine cycle.

In the accumulate mode, data is shifted out of the shift register by a shift-out pulse. Simultaneously, there is 1 μs pulse applied to the A/BSTROBEDØ line. This strobe pulse is, like the shift pulses, always present for each line. To accumulate data into the BCD counters, the count enable line (A/BCOUNTENAD1) is held true (high) and pulses are applied to the COUNTCLOCKD1 line. Each pulse causes the register to increment by 100. IC's 24, 25, and 26 are up/down BCD counters. In a normal accumulation operation, the strobe is followed by a single count-down pulse on the CDWNCLKD1 line. If this is the beginning of an accumulation, and the register had been previously loaded with zero's, then the count down pulses set the register to minus one hundred. Negative numbers are represented in 9's complement form. That is, after the count down, the

register will contain –99900 (which is equal to –00100 in sign-magnitude notation). The presence of a high TGATED1 will then cause the timing card to send out 16 MHz count-up pulses on the COUNTCLOCKD1 line. With the BIAS control on the input card set properly, a zero input signal from the vidicon will cause TGATED1 to be true for long enough to cause 100 count-up pulses, leaving the memory-counting register back at zero. A negative input signal will result in fewer up pulses, and, therefore, a negative number in the counting register. A positive input will result in a positive number.

The two low-order digits of the memory counting register only count up and are therefore normal "up-only" BCD counters. The circuit formed by the two flip-flops in IC-31 changes a negative transition from the output of the second digit to negative going pulses. The sign flip-flop (the cross-coupled gates of IC-36) is set positive by overflows of the most significant digit, and negative by underflows.

When accumulating, it is important to detect that the memory is at full scale. This is done by IC-34, whose output (A/BFULLDØ) goes low if any number is positive and has a nine in the MSD (most significant digit) followed by an 8 or a 9 in the second most significant digit.

In the store mode, the data is recirculated through the count register unchanged.

In the REAL TIME mode the memory in the shift register is retained but the count register is free to count the data from the present line only. This is done by resetting the counting register after the initial strobe as in an erase cycle, and introducing a second strobe at shift-in time. This second strobe again loads the data from the output of the shift register into the counting register in time for the data to be valid for the shift-in pulse.

Data is read out of the counting registers as five BCD digits by sequentially raising the TØD1-to-T4D1 lines. This occurs during the arithmetic cycle time which begins 8 μs prior to the shift-in pulse. These pulses are generated by the ARITHMETIC CARD and will be discussed in connection with that card. It is sufficient to note that the data is gated onto the A/BØ1BØ buss by 5 groups of 4 open-collector gates, and that the data is gated out serially by digits, LSD first. The sign is read out on a separate line.

10.4 ARITHMETIC CARD

The ARITHMETIC CARD handles the transfer of data from either memory to the output data registers, corrects negative data from 9's complement to sign magnitude, and subtracts the B memory data from the A memory data. The card also counts leading zeros in the data for the log mode.

Data is processed one BCD digit at a time, LSD first. Data from the A memory comes in on the AØ4BØ buss, and from B on the BØ4BØ buss. The results of an arithmetic process leave the card on the CØ4B1 buss.

The card generates its own timing signals. These signals are the T pulses (TØD1 to T4D1), AUCLOCKDØ, and CYCLE1D1.

When two signed numbers are subtracted serially by digit, it is not possible to anticipate which number should be the subtrahend and which the minuend. For this reason, a test subtraction must be performed to discover which number is the larger. To simplify the timing, all arithmetic processes are done twice, with only the results of the second operation being accepted as correct. The ARITHMETIC CARD has then two main cycles for each computation, cycle 1 to determine the proper direction of a subtraction, and cycle 2 to perform the operation. The A output of the bi-quinary counter IC-9 is set to a zero (low) for cycle 1 and to a 1 (high) for cycle 2.

Each cycle is divided into five parts, one for each digit in the five-digit words. This digit counting is performed by shift register IC-11. When all outputs of the shift register are low, output pin 8 of the four-input NOR gate 16 is high, indicating TØ time, that is, the time reserved for processing the 10° digit. At the end of TØ time, the shift register is clocked and a one is set at the output of of the first flip-flop of the four-bit shift register. This line is T1D1. Each successive clock moves the set bit to the next position in the register, generating T2, T3, and T4. It is the transition of T4D1 from high to low which toggles the cycle flip-flop in IC-9.

The "quinary" (divide by five) portion of IC-9 divides each "T" time into three parts. The first part of the T time is a 250 ns setup time, the second a 250 ns output data transfer time, and the third a 125 ns delay. Output data is valid slightly before and slightly after the middle "transfer" time. The middle timing pulse and cycle 2 are used to generate AUCLOCKDØ, which is used in combination with the "T" pulses to strobe the output registers.

The whole arithmetic cycle starts when the card receives an AUSTARTDØ pulse. This occurs after the end of the time when data is counted into the memories and 8 μs before a shift in pulse. The AUSTARTDØ pulse is also used to increment the line number and premark counters on the CURSOR card.

The AUSTART sets the $\overline{Q}$ output on pin 6 of IC-3 high. This releases the reset to the bi-quinary counter and shift register, and starts the cycle. The $\overline{Q}$ output of IC-3 pin 5 will go low at this time and set the $\overline{Q}$ output of the initialize flip-flop (IC-3, pin 3) high. This flip-flop will be reset by the first mid-digit time, approximately 250 ns later. The pulse thus generated is used to initialize the sign flip-flop (to a "plus"), the zero counter IC-6 (to a zero), and the carry flip-flop (to a "1").

The function of the ARITHMETIC CARD is determined by the three signals: REALSWDØ; ASWDØ; BSWDØ. The functions are: (1) Transfer and convert from 9's complement the data from the A memory; (2) Transfer and convert from 9's complement from the B memory; and (3) Subtract B from A.

The first mode is selected if either the REALSWDØ or the ASWDØ is low. The second mode is selected if BSWDØ is low. The third mode is selected if none of these lines is low.

The transfer operations are treated as subtractions with the data from the unwanted memory set to zero. It is therefore only important to explain the manner in which the unwanted data is set to zero and then to explain a subtraction.

IC's 17 and 18 are 4-bit logic elements. By manipulating the control lines B and C on pins 8 and 1, the device may: (1) Pass the data directly through, (2) Invert the data, (3) Pass out all zeros, and (4) Pass out all ones.

In the case of a transfer from A of positive data, IC-17 is commanded to invert the data, which brings it back to positive truth, and IC-18 is commanded to produce 1's. Since subtraction is performed by adding the 1's complement of the subtrahend to the minuend, this is equivalent to subtracting zero.

If the contents of A are negative, then IC-17 is set to transfer the data directly, which leaves it inverted, and IC-18 is set to produce zeros. This is equivalent to subtracting the A data from all nines and adding 1. The result is the sign magnitude number equivalent to the 9's complement number stored in A.

B transfers are accomplished in the same manner with the functions of IC-17 and IC-18 reversed.

As was mentioned above, if both numbers are positive, a subtraction is performed by adding the minuend to the 1's complement of the subtrahend. Unless there has been a borrow on the previous digit, the carry into IC-13 (an adder) is set. Take as an example the subtraction of 2 from 7. Seven in BCD is 0111 and two is 0010. So 0111 (7_{10}) is added to 1101 (the one's complement of 2_{10}) plus the carry-in bit. The result of this operation is 0101 and carry (not borrow). The presence of a carry causes all B inputs to the second adder (IC-12) to be low, and the result on the CØ4B1 buss is 0101, which is a BCD 5.

If the input numbers result in borrow's, then IC-12 comes into play. As an example, if A were 24 and B were 17, the first operation would be to add 4 to the one's complement of 7 plus 1 (the carry in).

$0100 = 4_{10}$
1000 = one's complement of 7_{10}
$\underline{\quad 1}$ = carry in bit
01101

The fact that a larger digit has been subtracted from a smaller is indicated by the lack of a carry at pin 14 of IC-13. This results in a 10_{10} being put on the B input of IC-12. The result of this addition is:

1101
$\underline{1010}$
$10111 = 7_{10}$ and a carry

The carry is ignored and 7 is placed on the CØ4B1 buss as the result for this digit. The carry flip-flop, IC-4, is also set to a zero. This results in a borrow from the next digit:

$0010 = 2_{10}$
1110 = one's complement of 1_{10}
$\underline{\quad 0}$ = no carry in
10000 = zero and no borrow

So our final result is 07.

When the number is negative, the two numbers are to be added, but because the negative number is in nine's complement form, addition is performed in exactly the same manner as above.

Only when both numbers have the same sign as above is it necessary to examine the results of the test subtraction (cycle 1) to determine the sign of the result and the proper direction of subtraction. This is done by assuming that the result will be positive, doing the subtraction, and then detecting whether the whole operation leaves a borrow. If it does, then the subtraction has been performed in the wrong direction and the correct answer will be negative.

During cycle 1, zeros are detected by IC-6 at ZEROD1. In the LOG mode, the binary counter, IC-6, is incremented for each zero digit. If a digit is zero, the counter is strobed with a zero. At the end of cycle 1, the counter will contain the number of zeros after the last significant digit. This number is used to select the digits fed into the three-digit DAC, and to determine the characteristic of the log. When not in the LOG mode, the output of the counter is strobed to the number set by the scale-factor switch.

10.5 OUTPUT CARD

The OUTPUT CARD generates the analog Y axis signals for the display oscilloscope and for the plotter.

The digital data from each channel is strobed into buffers IC-2, 6, and 9. The choice of the most significant digit for display is made by the DACE4, DACE2, and DACE1D1 lines. These lines control IC-1, which is an eight-input position scaler. If all of the S control lines are low, then T2 strobes IC-9, T3 strobes IC-6, and T4 strobes IC-2. This loads the 10^2, 10^3, and 10^4 digits into the buffer. If DACE1D1 is high, then 10^1, 10^2, and 10^3 are loaded. If DACE1D1 and DACE4D1 are low and DACE2D1 high, then 10^0, 10^1, and 10^2 are loaded. If DACE1D1 and DACE2D1 are both high with DACE4D1 low, 10^0, 10^1, and a zero are loaded. DACE4D1 high, DACE1 and DACE2 low, give 10^0 in the MSD and zeros in the other two digits. The DACE lines come from the ARITHMETIC CARD and are set by the scale switch on the front panel, or are set automatically for the LOG mode.

The DACE lines also go to the 6 bit DAC, IC-5, to generate a level equal to the characteristic (power of 10) of the input data for use in the log display.

The analog output of the three digit DAC, module 3, goes to the front-panel Vertical Expand adjustment and then

back to the output card. The return signal, DACA+, goes to a controllable inverter, IC-11, to multiply the signal by +1 or −1 to add the sign information. When MOS switch 10 (input pin 10) is closed, the operational amplifier inverts. When ARITHNEGD1 is high, the switch opens and the operational amplifier is a voltage follower and does not invert.

One side of MOS switch 10 (input pin 12) is used to switch the level of the analog signal applied to the current summing junction on pin 2 of IC-8. When LOGD1 is low, the switch is closed and the current into the summing junction from the output of IC-11 is the sum of the current through the switch and through R9 and R10. With the switch closed, the linear Position trimmer is functional and adds a dc bias to the signal for positioning.

When LOGD1 goes high, the switch opens and the signal due to the DAC is reduced by a factor of five. The position trimmer is also disabled. The LOGD1 signal also activates the exponent DAC, IC-5, by gating the DACE lines through to the input of the DAC. The output of the DAC is summed with the attenuated signal from the three-digit DAC, module 3. The result of the summation is the Y axis signal that appears on the rear panel as CRT Y and on the Display Card as SAMPLEYAN for use by the plotter sample-and-hold circuit. Diodes ZD1 and ZD2 clamp the CRT Y output at ±5 V.

10.6 INTEGRATE CARD

The INTEGRATE CARD holds the digital output register, the integration register, and control logic for integration. When not integrating, the output register (IC's 18, 19, 20, 21 and 22) is loaded from the CØ4B1 buss with the data for the channel selected by the cursor via the ENORD1 line. When integrating, the ENORD1 line is held low and data is counted into the register through the ORUPDØ and ORDOWNDØ lines. The integrate register (IC's 23, 24, 25, and 26) is strobed to load the data from the CØ4B1 buss for the cursor-selected channel. This data is then counted down to zero while the output register is counted up or down.

The direction of counting is determined by three things: (1) The sign of the number in the integrate register; (2) The sign of the number in the output register; and (3) The direction the cursor was moved. For example, if both numbers are positive and the cursor is moved to the right, the output register is counted up. The three terms are combined in the two exclusive OR gates in IC-13 with output lines 10 and 11.

When the integrate button is pressed, the two flip-flops in IC-5 and the NAND gate (IC-4 pin 1) give an initialized pulse INTRDØ. This pulse resets the control flip-flops and the output register.

The integrate register is strobed when the output of IC-9 pin 11 is high. This will happen when the channel corresponding to the CØ4B1 buss is the same as that selected by the cursor (i.e., CHMARKD1 is high) and the integrator is not busy counting down (i.e., RUND1 is low). AUCLOCKDØ is a timing signal which is low only when data on the CØ4B1 buss is valid.

When either the cursor-up or the cursor-down buttons are pressed, a pulse is created on either the CURSDWNDØ or CURSUPDØ lines. This pulse comes from the control card and occurs during the retrace interval. Either pulse initiates a run cycle. If the cursor up (right) button was pressed, then CUPD1 is set. The previous state of CUPD1 is shifted out to IC-6 pin 9. Normally, RUND1 does not set immediately. Instead, IC-8 is set on pin 9 and RUND1 will be set after the data from the new channel has been strobed into the integrate register. This is done by IC-7 pin 4 clocking the run flip-flop (IC-10 pin 11) during the loading of the integrate register following the cursor pulse. The rise of this pulse will set RUND1 high and reset IC-10 pin 9. If, however, IC-8 pin 4 is high after a cursor pulse, then a RUN cycle will begin immediately and data from the previous channel will be counted down. This can happen for two conditions; one is when an integration is started (the initialize pulse sets IC-8 pin 5). The second condition is when the state of CUPD1 and IC-6 pin 9 (the previous state of CUPD1) are different (this will occur when the direction of cursor motion is reversed).

Once RUND1 is set, a ring counter, IC-3, will start running. This counter generates a 500 ns IRDOWNDØ pulse, a 500 ns pause, then a 500 ns pulse during which the output register is counted up or down, and last, another 500 ns pause. The process stops when the integrate register reaches zero and an IRBORROWDØ pulse occurs. This resets the RUN flip-flop.

If a down pulse to the output register causes the contents of the register to go below zero, ORBORROWDØ will go low. This signal is fed to the clock of IC-17 (pin 11), which is the output register sign bit, and the sign is reversed. This causes the direction of counting to reverse. If the output register overflows, INTERRORDØ is set and the error LED on the front panel is turned on.

Since the integrate register does not contain the least significant digit, the result of an integration is always divided by at least 10. A divide by 100 is possible by raising the INTX10DØ line. This activates the up-down decade counter IC-1 and divides by 10 the number of pulses going to the output register.

10.7 DISPLAY DRIVE CARD

The DISPLAY DRIVER CARD generates the X and Z drive for the display oscilloscope, the slow X-axis ramp for the plotter, and contains the sample-and-hold for the plotter Y axis.

The X axis oscilloscope ramp is generated by an integrator (IC-3, output pin 7). The ramp rate is controlled by the front-panel horizontal expand pot. This pot produces a voltage ranging from 0 to −15 V and is connected to HOREXA-. In the calibrate position, the HOREXA- voltage is zero and the ramp rate is set by the X RAMP trimmer. The signal from the expand pot is filtered by C13 and is then used by the ramp generator and the Z axis circuit. The

ramp is reset by RCRTXDØ going low and closing the MOS switch in IC-4 (pin 12). In the calibrate position, the ramp is reset at the retrace time. In the expand mode the reset pulse occurs at the premark time. Premark is a pulse which precedes the channel mark time by approximately 700 μs.

The output for the display CRT Y axis from the output card is also connected to a sample and hold on the display drive card. The signal, SAMPLEYAN, is connected to the positive input of voltage follower IC-3. The input to IC-3 is clamped to zero by Q1, except when the PLOT/PRINT switch is depressed.

MOS switch IC-4, pin 10, is driven by MARKDØ and connects the output of the voltage follower to capacitor C11 when MARKDØ goes low. This happens during channel mark time, with a delay set by IC-1 to allow SAMPLEYAN to settle. The capacitor is connected to a second follower, IC-6, whose output is the PLOTY signal.

The plot ramp generator is an integrated circuit consisting of IC-7, C15, IC-5, and associated components. The ramp rate is set by the PLOT RAMP trimmer and by transistor Q2. When SLOWMODED1 is low, Q2 is on, and clamps the trimmer's output voltage to zero, causing the ramp to stop. Normally this will happen after the 499th channel has been plotted. When not in the plot mode, the P/PSWDØ level is high and MOS switch 5 (pin 12) is closed, resetting the plot ramp.

The output of IC-7 is divided by R37 and R38 to provide a lower output level and protection from external voltages.

The Z axis circuit generates a three-level signal to intensify and blank the display oscilloscope. There is a normal level set by the Z LEVEL trimmer. This trimmer sets a fixed current into the summing junction at pin 2 of IC-8, establishing the normal level at the output of IC-8 (pin 1). A one shot, IC-1, is triggered at the beginning of each arithmetic cycle by AUSTARTDØ, producing an ≈15 μs pulse while the output of new data is settling on the oscilloscope Y axis. This pulse is combined with FRBLANKDØ to produce a signal at IC-2 pin 13, which is high for the frame-blank time and for the settling time of the Y axis. This signal is converted to a current by the level-adjusting trimmer, Z BLANK, to produce a variable negative-going blanking signal at the output of IC-8 pin 1.

The output of IC-2 pin 1 is low for the marked channel (i.e., CHMARKD1 high) after the settling time. This signal closes the MOS switch IC-5 from pins 6 to 8 when low. When the switch is closed, a negative current is applied to the summing junction (IC-8 pin 2), providing a positive-going intensify pulse at pin 1 of IC-8. The level of this pulse is set by the Z MARK trimmer.

The filtered negative-going voltage from the HORIZ DISPLAY EXPAND control is applied to the Z COMP trimmer and then to the summing junction. This causes the output of IC-8 pin 1 to go more positive (i.e., in the direction of increasing CRT intensity) as the expansion is increased. This compensates for the decreasing writing time of the beam of the CRT. The trimmer is adjusted so that the expanded and non-expanded intensity are the same.

The output of IC-8 pin 1 is divided by R14 and R15 and sent out as CRT Z. The signal is also run through the polarity switch S1 to input pins 5 and 6 of IC-8. With the switch in the "+" position, IC-8 will have positive gain; in the "—" position, negative gain. The gain is set by the Z HIGH trimmer. This produces Z axis drive and CRT Z high, with up to 24 V of swing and with greater intensity in either the positive ("+" on S1) or negative ("—") direction.

10.8 CURSOR CARD

The CURSOR CARD contains three 3-digit counters and a three dual-4-bit comparator. The counters are the line number counter, the premark counter, and the cursor counter. The line number counter (IC's 4, 12, and 17) advances with every line scan and contains the line number for the channel presently available from the arithmetic card. The premark counter (IC's 3, 11, and 16) contains the present line number plus 12. The cursor counter is made up of 3 up/down counters that contain the number of the channel selected by the front-panel cursor controls for digital display. When the cursor counter and the line number counter are the same, the A outputs of the three comparators will all go high, causing CHMARKD1 to go high. The low-going reset pulse to the line number counter is ANDed with the output of the comparators to prevent spikes on CHMARKD1 during the reset.

The PREMARKD1 signal will go high 12 line-times in advance of the channel selected by the cursor counter.

FRBLANKD1 is high for line number 500 to 511. This is achieved by decoding the presence of a five (0101_2 in BCD) in the MSD of the line number counter. The output on pin 9 of IC-9 is set high by the rise of FRBLANKD1 and stays high until the presence of a 6 in the LSD of the line number counter (decoded by IC-15, pins 4, 5, and 6). This generates the frame retrace pulse FRRETRACEDØ and its positive going inverse, FREETRACED1. These signals are true for the interval from the rise of the line number 500 until the rise of line number 506.

IC-2 and the associated gates create pulses for synchronizing the premark counter and the line counter and for resetting the line counter at 512.

The cursor counter may be remotely programmed by lowering the LNSTROBEDØ line. In this state the counters will follow the data (cursor address) loaded on the PGMLN12B1 buss (PGMLN01D1 to PGMLN24D1). PGMLN28D1 is a spare for expansion to a 1024 channel system. Multiplexer IC-7 and flip-flop IC-8 provide a circuit which resets the counter to zero after 499 when counting up, and to 499 when counting down through zero. When LNSTROBEDØ is low, this function is, of course, disabled.

10.9 CONTROL CARD

The CONTROL CARD provides the control signals for most of the functions of the O.M.A.

A 16 MHz crystal oscillator drives a divide-by-16 counter (IC-18) to provide the time base for all circuits.

The flip-flops in IC-12 generate SLOMODED1, which is a signal that goes high when the PLOT/PRINT switch is pushed and goes low after the 500th channel has been plotted. Pushing the PLOT/PRINT switch causes P/PSWDØ to go low, releasing the reset to both sections of IC-12. The 1 MHz clock then sets SLOMODED1 high. ADR24D1 will fall when the channel address goes from 499 to 000, clocking IC-12 and setting SLOMODED1 low.

When in the slow mode (SLOMODED1 high), there are several ways of advancing the line number counter through the addresses. With the PLOT RATE switch (located on the back panel) set to a non-zero position, the line will advance after the selected number of machine cycles. When the PLOT RATE switch is set to zero, the cursor may be advanced by PLOTCMDØ or PRINTINHDØ as explained below. When in the slow mode and when IC-24 pin 9 goes high, IC-13 pin 6 goes low and loads the down counter, IC-22, with the number set by the PLOT RATE switch. When not in the slow mode, the counter is continuously strobed.

The counter is clocked by ORT2DØ, which is a strobe pulse for the 10^2 digit of the output register. The count down will continue until the counter is at zero and an ORT2DØ appears. This will cause the borrow output on pin 13 of the counter to go low, again setting IC-24 pin 9 high. The load pulse again sets the counter to a non-zero number and the borrow output of the counter goes high. The ORT4DØ line is the strobe to the 10^4 digit of the output register. This line goes low shortly after ORT2DØ, and resets the flip-flop IC-24 (pin 9 goes low). At the same time, the counter is being reset and IC-24 pin 8 is low. If SLOMODED1 is high, and PLOT RATE is non-zero, then IC-15 pin 8 will go high; IC-11 pin 13 low; IC-21 pin 13 high; and CURSUPDØ will go low. This will advance the cursor to the next channel. The ORT2 and T4 pulses occur when the output register is strobed with the cursor selected channel. Since the address has just been advanced by the end of the output register strobe, the next line to read out will be the newly selected channel. Sixty-three microseconds after the cursor advances, the data for that channel will be read into the output register. If the PLOT RATE had been set to 1, the load will count the counter down to 0. One frame later the borrow will occur causing a cursor advance, and again loading data.

If the PLOT RATE is set to zero, the NOR gate IC-23 will have a high on pin 6 and disable the automatic advance. There are, however, two other mechanisms for advancing the cursor.

The PRINTINHDØ and PLOTCMDDØ are a pair of lines for automatically advancing the cursor and supplying data to an asynchronous device. When SLOWMODED1 goes high, IC-12 pin 2 goes low, removing the reset from both flip-flops in IC-10. When the data from the first selected channel is loaded, ORT4DØ will set IC-10 pin 9 high, which will in turn set PRINT/PLOTCOMDDØ low. When the device attached to the 1205 detects this state, it should respond by lowering PRINTINHDØ. This will cause a reset to IC-10 pin 1 and remove the print command. When the device is through with the data, it should let the inhibit line (PRINTINHDØ) rise, causing IC-24 pin 6 to drop (provided the PLOT RATE switch is set to zero). When IC-21 pin 6 goes low, it will set the next flip-flop, IC-14 pin 5, and this will cause the cursor to advance, and will reset IC-14 pin 5 at the end of CHMARKD1. This process may be continued until channel 499 has been read out, after which SLOMODED1 will go low.

The cursor may also be advanced by pressing the cursor-right and cursor-left pushbuttons on the front panel. This may be done irrespective of the state of SLOMODED1.

IC-19 debounces the two cursor buttons. The rest of the circuitry between IC-19 and CURSDWNDØ and CURSUPDØ is devoted to generating a special pulse train. When a cursor button is pushed, there will be a single pulse to the CURSOR CARD at the next FRRETRACEDØ pulse. If the button is held down, there will be no more pulses for seven frame times and then there will be one pulse for every FRRETRACEDØ pulse. This allows the user to easily advance the cursor one channel or to move the cursor rapidly across many channels. The XOR, IC-20 pin 4, indicates that either button, but not both, have been pushed by going high. This will cause IC-14 pin 9 to set at the end of the next FRRETRACEDØ pulse. This releases the reset to the hexadecimal counter, IC-5. Pulses are enabled only when XOR IC-20 pin 3 is low. This condition exists when IC-14 pin 9 and IC-5 pin 12 are in the same state. The pulses are also gated by FRRETRACEDØ being low, IC-4 pin 5 being low, and only one cursor button pushed. The FRRETRACEDØ pulse that sets IC-14 pin 9 will therefore produce an up or down clock to the cursor, then for seven more clocks IC-14 pin 9 will be high and IC-5 pin 12 low. The eighth FRRETRACEDØ pulse will cause IC-5 pin 12 to go high and again enable pulses. When pin 12 goes high it also locks the counter clock in a low state stopping further counting.

The J-K flip-flop IC-4 controlling IC-15 pin 1 is used only in the integrate mode. When INTD1 is high and IC-5 pin 12 is high, the output goes high every other frame, reducing the cursor advance rate to 15 channels per second. This allows the INTEGRATE CARD time to process the data.

The circuit centered around IC-6 strobes the digital readout LED's on the front panel approximately twice per second (once per 16 frames) to allow the operator time to read the number when in the REAL TIME mode. This function may be locked out by opening the jumper on the REALSWDØ signal. When used, if REALSWDØ is low and the cursor buttons are not pushed, IC-15 pin 6 will go high, removing the strobe from the decade counter, IC-6. With no strobe, all output bits will be low once every 16 frames, strobing the LED's at those times.

The circuit around IC-1 generates a flag for a computer or other device for data transfers. It performs essentially the same function as the PRINTCMD and PRINTINH circuits but does not require that the PLOT/PRINT button be

depressed and does not alter the cursor. If DATAREQDØ is lowered by an external device, DATAREADYD1 will go high when the data for the cursor selected channel is loaded into the output register. Change of the data is then inhibited until DATAREQDØ is raised.

ENORD1, when true, enables the loading of data into the output register. AUCLOCKDØ is a timing signal indicating that the data from the ARITHMETIC CARD is valid. It is five 250 ns pulses every line time. The AND-OR-INVERT gate, IC-8 pin 6, selects between enabling the strobe on the cursor selected channel (CHMARKD1 high), or on the channel following the end of the frame retrace pulse. This channel contains the accumulation cycles count. The output register is disabled from strobing by INTD1 in the integrate mode during delay cycles when in the REAL TIME mode, and when DATAREADYD1 is high.

PRERESETDØ resets the preset counter if the PRESET HOLD switch is not depressed and if MRESETDØ goes low. MRESETDØ is low while either memory is being erased. The reset for memory erase is timed by IC-17 pin 8 to occur only for the line after the end of the FRRETRACEDØ pulse. This guarantees correct counting by the preset counter if a preset accumulation is reinitiated by pressing the MEMORY ERASE button.

RCRTXDØ is a signal which returns and holds the CRT X axis sweep at zero. This pulse normally occurs when FRBLANKD1 goes high; but if the expand control is not in the calibrate position, then EXPANDDØ goes low and the pulse occurs at PREMARKDØ time. PREMARKDØ is a pulse which precedes the channel mark pulse by 12 line times. By starting the CRT X sweep at the end of PREMARKD1, the expanded sweep will always start 11 channels ahead of the channel selected by the cursor.

SIGNORMDØ is a signal on the back panel for use by printers. It goes low to indicate that the data in the output register is from the memories and that it is not the result of an integration or an accumulation cycle readout.

10.10 TIMING CARD

The TIMING CARD generates the timing signals used to control the other cards in the O.M.A. The card also contains some control functions. The divider chain starting with IC-4 and ending with IC-2 divides the input 1 MHz signal by 64 and generates the Q1-to-Q6 clocks. For example, Q6 is a clock which is true for 2^6 μs. One cycle of Q6 is a line time. IC-2 pin 5 is the same frequency as Q6 but 90° out of phase.

When Q3, Q4, Q5, and Q6 are all high, IC-5 is reset on pin 10. This happens once each line time for 4 μs. Four microseconds after the reset, Q2 falls and sets IC-5 through the clock pin 9. This generates an 8 μs pulse LBLANK. RESINTD1 is the last 4 μs of this pulse and is used to reset the input signal up/down integrator. It is the end of this pulse which marks the beginning of the light measurement. The end of the measurement time is at the end of the sample time. SAMPLED1 goes high 4 μs before LBLANK and is gated off by LBLANK. Since the direction of integration is controlled by Q6, the integrate-up time and integrate-down time are equal, each being 28 (32–4) μs. The drive to the line scan is 90° out of phase with Q6 in order that the middle of the line be synchronized with the middle of the LBLANK pulse.

Shift register IC-10 divides the sample time into four 1 μs periods. The first of these is gated on the rise of SAMPLED1. Since IC-10 pin 13 is high as a result of the previous load command at the mode control (IC-10 pin 6), IC-12 pin 4 will go low, starting a SHIFTINDØ pulse. This pulse will end when the 1 MHz clock of the shift register moves the "on" bit to the B output, IC-10 pin 12, causing a 1 μs pulse to ASTROBEDØ, BSTROBEDØ and SHIFTOUTDØ. The next 1 MHz clock will end these pulses and start a CLEARTIMED1 pulse which is gated with the conditions of the memory erase buttons to clear the memories. The next 1 MHz clock will drop CLEARTIMED1 and raise IC-10 pin 10. If FRRETRACEDØ is high and the switch, S1, is in the 100 MEMORY OFFSET position, a single 1 μs pulse will appear at CDOWNCLKD1. During frame retrace, this pulse is eliminated. If S1 is in the MEMORY OFFSET 400 position, four cycles of the 4 MHz clock are gated to the CDOWNCLKD1 line. In either case, IC-10 pin 10 will fall at the same time as SAMPLED1.

The four 1 μs pulses are used to time the memories. SHIFTINDØ causes a clock to the shift registers which stores the data from the counting registers in the shift register. SHIFTOUTDØ causes a clock to the shift register that moves new data out from the shift register onto the parallel load lines of the counting registers. ASTROBEDØ strobes the A memory counting register and BSTROBEDØ strobes the B memory counting register.

In the REAL TIME mode, the A memory counting register is used to count the data for the present frame only. This is done by erasing the A memory counting register during the clear time and then restrobing the register with the shift register data during the shift in pulse. In this manner the data in the A memory shift register is retained, while the A memory counting register is freed to perform the counting for the real time mode.

The clear time pulse is the time during which the memory counting registers may be reset.

The CDOWNCLKD1 pulse counts the memory counting register down by one hundred or four hundred, prior to counting up, when the memory is accumulating. Normally, a zero analog input level will produce 100 up pulses, cancelling the effect of the count down 100 pulse. The count enable line on the MEMORY CARDS disable this pulse when not accumulating (CDOWNCLKD1 is enabled to memory A in real time also).

The TGATED1 signal from the input card, gated off during the SAMPLEDØ pulse, and synchronized with the 16 MHz clock, is present at Flip-Flop 20 pin 6. The input to the set terminal of the flip-flop gates this signal off during the frame-blank and delay-blank intervals. INBLANKD1 is the

FRBLANKD1 pulse shifted forward in time one channel to account for the delay from the input to the output of the 1205. When channel zero is on the XY display, channel one data is being digitized, and channel two data is being read from the vidicon. The synchronized TGATED1 signal is then gated by the 16 MHz clock to produce a 16 MHz pulse stream to COUNTCLOCKD1 while TGATED1 is high.

If the TGATED1 signal is still high at AUSTART time (when IC-11 pin 2 goes low), then the input signal is saturating the A-to-D converter. If this condition occurs, then IC-19 pin 10 will go low, setting flip-flop IC-20 pin 9 high. This will cause the error LED on the front panel, driven by ERRORLEDDØ, to turn on. IC-20 pin 9 will be reset by IC-11 pin 6 going low and then high after two FRBLANKD1 pulses. This guarantees that the error LED will be on long enough to be seen.

AUSTARTDØ is a signal which starts the arithmetic cycle when it goes low. IC-11 pin 2 will go low when Q5D1 and Q6D1 both go true, causing a clock. The flip-flop will reset 500 ns later when the 1 MHz clock goes high.

The memory-erase signals are synchronized with the frame-blank signal to guarantee that an erase cycle lasts for one entire frame. The REAL TIME signal button is also treated as an erase to the A memory, as previously explained, and is also synchronized to the frame blank signal. In the case of the A memory erase, if either synchronized signal to IC-15 pin 5 or 6 goes low, IC-15 pin 4 will go high. When the 1 μs CLEARTIMED1 signal goes high, a 1 μs low pulse will be placed on the AMEMERASEDØ line, causing a reset to the A memory counting register. This process will be repeated for at least the 512 lines of one frame. A similar series of pulses will be generated on BMEMERASEDØ if the B MEMORY ERASE button is pushed. Because of the synchronizing flip-flops, the erase commands (A/BMEMERSWDØ) must be low for longer than one frame time (32 ms), or they must be low when FRBLANKD1 goes high, to guarantee an erase.

If either memory is erased, MRESETDØ will go low and reset the preset counter.

If the A memory contains a number greater than 98,000 at AUSTARTDØ time, it is considered to be at full scale, AFULLDØ will be true, and flip-flop IC-6 pin 6 will go low. This pin will stay low until the memory is erased. If an accumulation to A is in process, AACCUMSWDØ will also be low and IC-23 pin 11 high, lighting the full scale LED through FSLEDDØ. If the FULL SCALE HOLD switch is depressed, FSHOLDSWDØ will be low and a full scale from the memory being used will halt the accumulation. The B memory full scale signal is treated in an identical manner through IC-23, 24, and 25.

An accumulation is enabled primarily by the A or B count enable lines. These lines are controlled by several conditions. First, there is a synchronizing flip-flop for each memory. In the case of accumulation to A, IC-16 pin 6 must be high during the fall of FRRETRACED1 to set IC-17 pin 5 high. This condition would normally occur on the first frame retrace after the A ACCUMULATE button is depressed. The start will not occur if AOPTHOLDD1 is high (possible only if the jumper to ground on this line has been cut) or if the A memory is at full scale and FULL SCALE HOLD is depressed. An accumulation will stop if any of the above conditions change and there is a rising pulse to IC-17's clock, pin 3, or if PREHOLDDØ goes low. PREHOLDDØ will go low during a clear time in the frame retrace interval if the PRESET HOLD switch has been depressed and there is a low level on PRECOMPD1 from the preset card. The clock inputs to the flip-flops of IC-17 go high once for each accumulation cycle, which corresponds to the completion of the selected number of delay cycles and the associated active vidicon read cycle.

With IC-17 pin 5 high, or upon selection of the real time mode, ACOUNTENAD1 will be high, enabling up and down counts to the A memory. With the exception of the real time mode, IC-17 pin 9 performs the same function for the B memory. These flip-flops also control the A and B LED's on the front panel to indicate that an accumulation to A or B is in progress. If either flip-flop is set, HOLDD1 will be low. If HOLDD1 is low or if REALTIMEDØ is low, IC-18 pin 4 will be high, enabling the delay counter by dropping DELINHD1.

The VBLANKD1 signal, when high, will cause the vidicon beam to be blanked. This will happen if any of the signals to IC-7 pins 5, 4, 3, or 2 are low. Normally, the beam is blanked for the frame retrace (FRRETRACEDØ low) and for delay blank cycles. The vidicon may also be blanked by the optional control line OPTBLANKDØ, or during the down half of the up/down integration of the signal from the vidicon, by placing switch S2 in the off position (thus inhibiting the dark current subtraction). Switch S2 is used to suppress dark current subtraction and use the entire face of the vidicon for accumulation if so desired.

10.11 PRESET

The PRESET CARD contains the delay cycle counter (IC-13), the four decades of preset counters (IC's 8, 2, 5, and 11), and their associated comparators. The delay counter counts frame times for which the vidicon is to be blanked prior to readout. The number of delay cycles may be set by the digital switch on the front panel to be between 0 and 11. The BCD output of this switch is connected to the A inputs of the dual comparator, IC-14. When the counter and the switch contain the same digit, IC-14 pin 7 will go high. The B inputs are for remote programming of the delay. When the digit represented in BCD by the state of the PGMDEL4B1 buss is the same as the counter, IC-14 pin 9 will go high. The same function is performed by the four comparators attached to the preset counter. The "and" outputs of the comparators on pin 7 of IC's 9, 3, 4 and 10 will go high only when all digits of the counters match with all of the digits of the switch on the front panel. The outputs of the comparators on pin 9 will all go high only when all digits on the PGMPRE16B1 buss match with the counters.

The delay counter is held reset to zero by DELINHD1. This signal will go low after the start of the frame retrace pulse at the beginning of an accumulation (or real time mode).

The counter is incremented and the output of the comparator sampled at the end of the frame blank interval. If DELPGMDØ is not pulled low by an external device, the comparison will be with the front panel switch. If the DELPGMDØ line is low, the comparison will be with the PGMDEL4B1 remote program buss. If, in either case, the comparison is with a zero, then flip-flop IC-6 pin 5 will have been set high by the previous FRBLANKD1 pulses. If the compare is with a one, then it will be the second FRBLANKD1 pulse which will set high IC-6 pin 5. This blank pulse will rise after one complete machine cycle, during which DELBLANKD1 will have been high.

With a DELAY other than zero, IC-6 pin 5 will go high after the selected number of delay machine cycles. When IC-6 pin 5 goes high, it will reset the delay counter, and the next FRBLANKD1 pulse will reset IC-6 pin 5. The machine cycle which occurs while IC-6 pin 5 is high is an active scan cycle, and during this time, the vidicon is unblanked and an accumulation to memory is performed. Unless the remote programming line SDELAYDØ is lowered, the rise of IC-6 pin 5 will lower DELBLANKD1 and IC-7 pin 9, and (since HOLDD1 is low during accumulation) will result in a pulse (which will fall on the rise of the next FREBLANKD1) to the Preset Counter, IC-8 pin 8. The Preset Counter will advance one at the end of each active scan (unblanked machine cycle).

If the compare is with a zero, IC-6 pin 5 will be high all of the time, DELBLANKD1 will always be low, and the Preset Counter will count each frame.

If SDELAYDØ is lowered by an external device, the functioning of IC-6 pin 5 is taken over by the DELBLANK2DØ and the PRECLOCK2DØ lines. These lines are for remote programming of delays longer than those which can be obtained internally, as when the 1205A is used with a 1207 extended delay accessory.

A memory erase to either memory, or the release of the PRESET HOLD button, will cause PRERESETØ to go low and reset the Preset Counter. If an accumulation is then started, the counter will increment at the beginning of the frame blank interval after each active machine cycle. If the remote program line PREPGMDØ is not lowered, the output of the counters will be compared with the front-panel switches and PRECOMPD1 will go high on a match. If PREPGMDØ is lowered by an external device, then the compare will be with the data on the PGMPRE16B1 buss.

The foregoing assumes that the PRESET CARD switches S1 and S2 are in the "normal" (right-most) positions. With these switches in the "reverse" positions, the functions of the front-panel DELAY and PRESET switches will be interchanged.

10.12 LINE SCAN

The LINE SCAN CARD accepts a digital signal, V. LN DRIVEDØ, and generates a square wave to drive the line-scan coil on the output named LS OUT AN. The L. SCAN trimmer sets the amplitude of this signal. With switch S1 in the CENTER position, the signal is amplified by the NE531V operational amplifier and the emitter followers, Q2 and Q3, and capacitively coupled to the output. With switch S1 in the ADJUST position, the output is resistively coupled and trimmer R8, labeled L. POSN for line position, adjusts the dc offset of the line scan.

Transistor Q4 is part of a protection circuit which blanks the vidicon if either scan signal is not present. This prevents a stationary electron beam from burning the target of the vidicon.

As long as there is an ac signal at L.S. OUT AN, Q4 will be turned on often enough to keep capacitor C14 below a logical zero and, therefore, keep L. PROTD1 not true.

It should be noted that the square wave voltage output of the line scan card causes a triangular current waveform in the inductive line-scan coil.

10.13 FRAME SCAN CARD

The FRAME SCAN CARD generates a sawtooth wave for the frame scan coil. The vidicon frame retrace signal (VFRETRACED1), when true (high), causes transistor Q1 to clamp capacitor C7 to zero volts. When this signal goes low, Q1 will turn off and C7 will charge linearly due to the current from resistor R2.

This process of repetitively clamping C7 once each frame will result in a 32.8 ms sawtooth wave on C7. This signal is directly coupled to a second op. amp. with gain trimmer R7, labeled F. SCAN. A dc offset is set by the trimmer R4, labeled F. POSN. This trimmer is normally set to give minimum dc bias to the signal at the output.

A third op. amp., together with resistors R10, R12, R13, and R15 provide a precise sawtooth current into the frame scan coil at FRS OUT AN.

Transistor Q2 is ac coupled to the frame scan output and will keep capacitor C11 discharged as long as there is a frame scan signal. F. PROTD1 will go true (high) if the frame scan signal is not present.

10.14 BLANKING, ALIGNMENT AND FOCUS CARD

The BLANK, ALIGN, FOCUS CARD generates the blank signal to the vidicon cathode, the alignment current for the line and frame alignment coils, and the current for the focus coil.

If any, or all, of the signals F. PROTD1, L. PROTD1, or V. BLANKD1 go high, NOR gate 1 will go low at pin 6 and high at pin 8. This signal will cause Q1, and therefore Q3, to turn off, driving V. CATAN (cathode voltage) to +15 V. If none of the above signals are high, Q1 and Q3 will be on. V CAT will be at a voltage between 0 V and −15 V set by trimmer R13 labeled CATH. A normal level for this voltage is −6 V.

Trimmer R3 labeled L. ALN establishes a current through R1 and therefore the line alignment coil at L. ALN AN. This coil in the 1205B aligns the electron beam in the vidicon in the "line" (as opposed to frame) direction.

Trimmer R4 labeled F. ALN establishes a current through R2 and therefore the frame alignment coil at F. ALN AN. This coil in the 1205B aligns the electron beam in the vidicon in the frame direction.

A regulated current for use in the vidicon focus coil is generated at FOCUS I AN. Transistor Q2 is operated as an emitter follower with a temperature compensated voltage on its base. Trimmer R10 (labeled FOC. 1) sets the current at the collector of Q2. Resistor R14 and C7 provide noise filtering.

10.15 HIGH VOLTAGE CARD

The HIGH VOLTAGE CARD, located on the SYSTEM POWER BOARD, supplies the four high voltages for the vidicon. The highest voltage, G4, is shunt regulated by Q1, which in turn is driven by the 5741 op. amp. The op. amp. compares the voltage divided from G4 by R10, R11, and R12, with the voltage on trimmer R3, derived from the +15 V supply. R3 (labeled G4) adjusts the G4 voltage and therefore also changes the voltages derived from G4, that is, G3 and G2. G4 is normally set at +340 V. Trimmer R10, labeled G3, may then be set to give 290 V at G3, and R8 may be set to give 300 V at G2. Trimmer R2, labeled G1, divides a negative voltage regulated by ZD1, and should be set to give approximately −70 V at G1. These voltages are available at testpoints TP1 to TP4.

10.16 VIDICON PREAMP BOARD

The VIDICON PREAMP BOARD contains the low-noise vidicon preamplifier. The low-level signal from the vidicon target is connected through a short wire to the input of a high performance FET input operational amplifier. The input op. amp. is wired as an integrator with the addition of a high impedance dc negative feedback. The output of the integrator is ac coupled to a second op. amp. which is essentially a differentiator. (The net result of the two feedback circuits is to put the "pole" of the second op. amp. on top of the "zero" of the input op. amp. in the complex frequency plane.) The whole circuit works as a current-to-voltage converter, with the output signal present at VIDSIGAN. Trimmer R2 is used to zero the offset bias of input op. amp. to zero. Trimmer R10 is used to adjust the clamp level at the second stage input, thereby increasing the DELAY range.

10.17 LOW VOLTAGE POWER SUPPLIES

There are four low voltage power supplies located on the SYSTEM POWER BOARD. The supplies provide regulated output at +5 V, +15 V, −15 V, and −6.2 V. All low voltages have their own series pass regulator.

The +5 V supply will handle up to 5 A through a Darlington pass transistor driven by a μA723 regulator. The +5 V output is trimmed by the +5 V ADJ trimmer R2. Resistor R6 sets the level at which the regulator will current limit to approximately 6 A.

Devices A2 and A3 are complete 15 V regulators. Each will provide 600 mA before going into a thermal current-limit mode, or falling out of regulation.

The −6.2 V filament supply is series regulated by zener ZD1 in conjunction with emitter follower Q1, and will provide up to 200 mA of filament current.

SECTION XI
SIGNALS

11.1 MNEMONICS

11.1A INTRODUCTION

Mnemonics are used for identifying signal lines and busses to provide a terse and easily remembered name for these lines. This assist to communication is of value where the design is done by blocks, and these blocks are usually defined in terms of their inputs and outputs.

11.1B MNEMONIC STANDARDS

(1) Character Set

Only upper case letters, the digits "Ø" to "9", and the following special characters are allowed:

. / + –

Spaces are not allowed. The number zero is written Ø to remove ambiguity with the alphabet letter O.

(2) Number of Characters

Mnemonics may have up to fifteen characters. Those with less are considered to be right justified.

(3) Last Two Characters

The second from the last character shall be either B, D, A, or V.

"B" signifies that the mnemonic is for a buss. The last character may then be 1, Ø, N, or A where 1 signifies digital positive truth, Ø signifies negative truth, N signifies that there is no truth value assignable (polarities are mixed), and A signifies an analog buss.

"D" signifies a digital line. When used it must be followed by 1 or Ø to signify positive or negative truth.

"A" signifies an analog line. This character should be followed by +, –, or N. + is used to identify positive going analog signals, – is used for negative analog signals, and N for Not Applicable (analog signals which go positive and negative).

"V" signifies a power line. V is followed by +, –, or A where + is for a positive dc supply, – for a negative supply, and A for ac supplies.

(4) Busses

For mnemonics ending in B1, BØ, BN or BA, the two characters before the B are the decimal number of lines in the buss.

For lines that are members of a buss, the third and fourth characters from the right are numbers which identify the line. The remaining characters for a line in a buss are the same as for the name of the buss. The numbers will have special significance for busses with binary or BCD data. For binary lines the numbers will be the exponent of the power of two, signified by the line. For BCD, the first digit will be the power of ten and the second 1, 2, 4, or 8.

Example: BCDØ8B1 is the name of a buss with 8 lines in it. All lines have positive truth. BCDØ1D1 is the name of the least significant bit in the above buss. It has positive truth.

(5) Power Lines

For all lines ending in V+ or V–, the previous characters give the voltage.

Example: 5V+ is a 5 volt power line; 3.2V– is a negative 3.2 volt power line.

(6) Uniqueness

The same may not be used for two lines which are not connected by a conductor. For cases where a signal is run through two inverters, the output signal must have a name different from the input signal. For this purpose, the old mnemonic must be modified by the addition of a number and a slash.

Example: INPUTD1 1/INPUTD1

11.2 SIGNAL GLOSSARY

1MHZD1	1 MHz Clock
2MHZD1	2 MHz Clock
4MHZD1	4 MHz Clock
8MHZD1	8 MHz Clock
16MHZD1	16 MHz Clock
AØ1DØ	A memory output buss 1 bit – 1×10^X weighted bit of A memory digit-serial output buss.
AØ2DØ	A memory output buss 2 bit – 2×10^X weighted bit of A memory digit-serial output buss.
AØ4DØ	A memory output buss 4 bit – 4×10^X weighted bit of A memory digit-serial output buss.
AØ8DØ	A memory output buss 8 bit – 8×10^X weighted bit of A memory digit-serial output buss.

AACCUMSWDØ — A memory ACCUMULATE switch — Input control switch enables accumulation into A memory.

ACCUMCYSWDØ — ACCUMULATE CYCLES switch — When ACCUM CYCLES switch is pressed, this line enables transfer of # of accumulate cycles associated with selected memory into output register.

ACOUNTENAD1 — A memory COUNT ENABLE — Gates on COUNTCLOCKD1 and CDOWNCLKD1 inputs to memory A.

ADR12B1 — Channel Address Buss — A 12 wire, 3 BCD digit data buss carrying the address (Line Number) of the cursor-selected memory channel.

ADR24D1 — Channel Address Buss — 10^2 digit 4 bit line, 400 weighted line of address buss ADR12B1.

AFULLDØ — A memory FULL — Low if the A memory counter contains a number +98000 or greater.

ALEDDØ — A memory accumulate L.E.D. — Lamp lights when accumulating into memory A.

AMEMERASEDØ — A MEMORY ERASE — Erases A memory by clearing A memory counter during each channel for one or more frames. During real time mode, clears stored number temporarily from counter.

AMEMERSWDØ — A MEMORY ERASE switch — On front panel - also operated by input card power-on reset and by remote program.

ANEGD1 — A memory NEGATIVE — High if the current A memory channel intensity (in the counter) is negative.

AOPTHOLDD1 — A OPTIONAL HOLD input — Cutting ground jumper on TIMING CARD enables this additional "A Accumulate" hold input for option applications.

ARITHNEGD1 — ARITHMETIC output is NEGATIVE — Indicates sign bit associated with data on arithmetic output buss "C".

ASTROBEDØ — A memory STROBE — Enters next channel data into A memory Counter from A memory shift register after arithmetic cycle. Operated during SHIFTOUT and, in REAL time mode, reloads previous channel prior to SHIFT IN.

ASWDØ — Display Select A switch — Low when A memory display is selected on front panel or programmed from digital output connector.

AUBUSYD1 — Arithmetic Unit BUSY —High during 6.25 μs arithmetic cycle.

AUCLOCKDØ — Arithmetic Unit Clock — Five pulses centered in the second set of TØD1 through T4D1 pulses in each arithmetic cycle indicate valid arithmetic outputs on "C" buss.

AUSTARTDØ — Arithmetic Unit Start — Pulses initiate 6.25 μs arithmetic cycle for each channel.

BØ1DØ — B memory output buss 1 bit — 1 x 10^X weighted bit of B memory digit-serial output buss.

BØ2DØ — B memory output buss 2 bit — 2 x 10^X weighted bit of B memory digit-serial output buss.

BØ4DØ — B memory output buss 4 bit — 4 x 10^X weighted bit of B memory digit-serial output buss.

BØ8DØ — B memory output buss 8 bit — 8 x 10^X weighted bit of B memory digit-serial output buss.

BACCUMSWDØ — B memory ACCUMULATE input control switch — Input control switch enables accumulation into A memory.

BCOUNTENAD1 — B memory COUNT ENABLE — Gate COUNTCLOCKD1 and CDOWNCLKD1 inputs to B memory.

BFULLDØ — B memory FULL — Low if the B memory counter contains a number +98000 or greater.

BLEDDØ — B memory accumulate L.E.D. — Lamp lights when accumulating into memory B.

BMEMERASEDØ — B MEMory ERASE — Erases B memory by clearing B memory counter during each channel for one or more frames.

BMEMERSWDØ — B MEMory ERASE switch — On front panel - also operated by input card power-on reset and by remote program.

BNEGD1 — B memory NEGATIVE — High if the current B memory channel intensity (in the counter) is negative.

BOPTHOLDD1 — B OPTIONAL HOLD input — Cutting ground jumper on TIMING CARD enables this additional "B Accumulate" hold input for option applications.

BSTROBEDØ — B memory STROBE — Enters next channel data into B memory counter from B memory shift register after arithmetic cycle during SHIFTOUT time.

BSWDØ — Display Select B switch — Low when B memory display mode is selected on front panel or programmed from digital output connector.

CØ1D1 — "C" Buss 1 bit — 1 x 10^X weighted bit of digit-serial arithmetic output buss.

CØ2D1 — "C" Buss 2 bit — 2 x 10^X weighted bit of digit-serial arithmetic output buss.

CØ4D1 — "C" Buss 4 bit — 4 x 10^X weighted bit of digit-serial arithmetic output buss.

CØ8D1 — "C" Buss 8 bit — 8 x 10^X weighted bit of digit-serial arithmetic output buss.

CDOWNCLKD1 — Count memory DOWN CLocK — Decrements memory 100 or 400 counts to compensate for input A/D bias.

CHMARKD1 — CHannel MARKer pulse — 64 μs pulse coincides with output of selected channel.

COUNTCLOCKD1 — A/D output pulse train — A burst of 16 MHz clock pulses proportional in number to the input voltage on the corresponding channel. Increments that channel in enabled memory counter.

CRTX — CRT display X axis drive — An analog sweep ramp for X-Y scope displays.

CRTY — CRT display Y axis drive — Vertical deflection voltage for X-Y scope displays.

CRTZ — CRT display Z axis drive — An analog intensity/blank signal for standard scope display.

CRTZHIGH — CRT display Z axis drive — An analog intensity/blank signal with amplitude and sense adjustable for non-standard scope display.

CURSDWND0 — CURSOR count - DOWN clock — Cursor counter/address register decrements on thepositive-going edge of clock pulses on this normally high line.

CURSUPD0 — CURSOR count - UP clock — Cursor counter/address register increments on the positive-going edge of clock pulses on this normally high line.

DACA+ — D/A Converter output — Signal after VERT DISPLAY EXPAND switches and attenuators.

DACCALA+ — D/A Converter output Calibrated — Provides standard vertical gain factor in "CAL" position of VERT DISPLAY EXPAND control.

DACE1D1 — D/A Converter Exponent 1 bit — 1 weighted bit of 3-bit D/A Converter exponent control buss. Shifts D/A converter input 1 BCD digit.

DACE2D1 — D/A Converter Exponent 2 bit — 2 weighted bit of 3-bit D/A Converter exponent control buss. Shifts D/A converter input 2 BCD digits.

DACE4D1 — D/A Converter Exponent 4 bit — 4 weighted bit of 3-bit D/A Converter exponent control buss. Shifts D/A converter input 4 BCD digits.

DACOUTA+ — D/A Converter Output — Direct output from 3-digit D/A Converter.

DATAREADYD1 — Handshake signal — Comes up in response to DATAREQD0 when the next transfer of new data into the output register is completed. Inhibits further changes in output register until reset by releasing DATAREQD0.

DATAREQD0 — DATA Request - Handshake signal — Enables DATAREADYD1 flag when low, resets DATAREADYD1 when high.

DELBLANKD1 — DELay BLANK — Blanks vidicon beam and inhibits COUNTCLOCKS and CDOWNCLK for a selected number of frame times per frame scanned.

DELBLANK2D0 — DELay BLANK #2 — Delay Blank input used by EXTENDED DELAY OPTION.

DELINHD1 — Delay Inhibit — Holds the delay blank counter at zero when not accumulating or, in REAL TIME mode, to insure starting in correct phase.

DELPGMD0 — Enable DELAY PROGRAM — Enables remote program input when low. Activates PGMDEL4B1 program buss instead of delay switch.

DIFFSWD0 — DIFFERENCE SWITCH — Low in the "A—B" Display select mode.

DIGNEGD1 — DIGITAL output is NEGATIVE — The sign bit of the digital output register. High when the number on DIG20B1 is negative.

DIG20B1 — Digital output Buss — A 20-line, 5-digit BCD buss carrying the digital data from the output register.

ENLEDSD0 — Enable L.E.D. numeric displays — Reduces readout rate to 3/sec in real time mode by disabling readout strobe.

ENORD1 — ENable Output Register — Enables ORT0D1 through ORT4D1, allowing transfer of selected channel data into output register.

ERRORLEDD0 — ERROR Light Emitting Diode — Lamp on numeral card between address and magnitude lights up if: (1) Input overload (2) Integrate overflow (3) Optional error signal.

EXPANDD0 — Horizontal EXPAND control — Low during Horizontal EXPAND mode on scope display.

FRBLANKD1 — Frame BLANK — The 12 channel (x 64 μs) blank interval - displays blanked, no data in channels except # ACCUM CYCLES.

FRRETRACED0 — Frame RETRACE — First 6 channel times of 12 channel (64 μs/channel) FRAMEBLANK interval - vidicon retrace time, gates ACCUM CYCLE clocks into 1st 6 blanking interval memory channels.

FSHOLDSWD0 — Full Scale HOLD switch — When depressed, prevents further accumulation in either memory if a selected memory has reached +98000 or greater in any channel.

FSLEDD0 — Full Scale Light Emitting Diode — Illuminates FULL SCALE lamp if a memory selected by AACCUM or BACCUM input has reached +98000.

HOLDD1 — Accumulate Control Signal — High when not accumulating into either memory. Prevents incrementing preset counter and erases vidicon continuously if not in REALTIME mode.

HOREXA— — Horizontal Expand amplitude — A negative voltage proportional to desired horizontal (X axis) expansion of CRT display - increases CRTX ramp rate and compensates brightness by increasing CRTZ level.

INBLANKD1 — Input BLANK — Inhibits COUNTCLOCK during input channels associated with FRBLANK.

INTD1 — INTEGRATE mode control — High when in PEAK INTEGRATE mode.

INTERRORDØ — INTEGRATE ERROR — Indicates overflow in peak integrate mode - lights error LED.

INTSWDØ — Peak Integrate switch — Low when switch is depressed.

INTX1ØSWPØ — Peak Integrate X10 mode switch — Switch on back panel selects X10 or X100 mode in peak integrate. This line is low in the X10 mode.

LEFTSWDØ — CURSOR LEFT (←) switch — Normally open side of (cursor) switch. Low when ← INTEGRATE switch is pressed.

LEFTSWD1 — CURSOR LEFT (←) switch — Normally closed side of (cursor) switch. High when ← switch is pressed.

LNADVCLKDØ — Line Number Advance Clock — A low pulse on this line advances the cursor (line number).

LNSTROBEDØ — Line Number STROBE — When low sets the address register/cursor counter to the number programmed on PGMLN12B1 input buss.

LNZERODØ — Line Number ZERO — Low level resets address counter/register to channel zero. This line is set low by front-panel 0 control, power-on reset, or remote program.

LOGD1 — LOG control signal — High when LOG display mode is selected.

LOGSWDØ — LOG display select switch — Low when LOG display mode is selected.

MRESETDØ — Memory RESET — Low if either memory is being erased. A clear input to PRESET counter.

OPTBLANKDØ — OPTional vidicon BLANK — Extra vidicon blanking input for option applications.

ORTØDØ — Output Register Transfer — $1Ø^{0}$ digit, transfers least significant digit into output register.

ORT2DØ — Output Register Transfer — $1Ø^{2}$ digit, transfers third (x 10^{2}) digit into output register; also advances PLOT RATE counter.

ORT4DØ — Output Register Transfer — $1Ø^{4}$ digit, transfers most significant digit (x 10^{4}) into output register.

PGMDEL4B1 — Program Delay input buss — A 4-wire, 1-digit BCD data buss to remotely program the integration delay setting activated by DELPGMDØ.

PGMLN12B1 — Program Line Number buss — A 12-wire 3-digit BCD data buss to remotely program the address register cursor counter. LNSTROBEDØ sets the address register to the line number on this buss.

PGMPRE16B1 — Program Preset input buss — A 16-wire 4-digit BCD data buss to remotely program the PRESET hold setting. Activated by PREPGMDØ.

PLOTCMDDØ — See PRINT/PLOTCMDDØ.

PLOTNULLD1 — Plotter null signal — An optional connection to PRINTINHDØ line for incremental plotter applications. Plotter generates PLOTNULLD1 when plot point is completed, advancing cursor in SLOMODE if plot rate = zero.

PLOTX — Plotter X-axis drive — A slow ramp during SLOMODE to drive plotter X-axis sweep.

PLOTY — Plotter Y-axis drive — Sample and hold output delivers Y-axis (vertical) output for plotter.

P/PSWDØ — Plot/Print switch — Low when Plot/Print switch is pressed.

PRECLOCK2DØ — Preset counter CLOCK #2 — Clock input to preset counter when EXTENDED DELAY option is activated.

PRECOMPD1 — Preset Compare — Indicates preset counter has counted the number of accumulated cycles selected by PRESET thumbwheel or remote program.

PREHOLDSWDØ — Preset HOLD switch — When pressed, inhibits memory accumulation when preset number of accumulate cycles have taken place. Zeros preset counter when released.

PRELEDDØ — PREset Hold Light Emitting Diode — Lights up if memory accumulation is being inhibited by preset hold circuitry.

PREMARKD1 — PREtrigger for channel MARK — A pulse 12 channels prior to the selected channel, CHMARKD1. Used to provide a pre-trigger for expanded CRT displays.

PREPGMDØ — PREset ProGraM input — Remote program input which, when low, activates PGMPRE16B1 program inputs instead of PRESET thumbwheel.

PRERESETDØ — PREset hold counter RESET — Zeros PRESET counter if PRESET HOLD is released or a memory is erased.

PRINTCMDDØ — See PRINT/PLOTCMDDØ.

PRINTINHDØ — PRINT Inhibit — Low level from printer indicates printer has received PRINT COMMAND and is busy printing. Resets PRINTCMDDØ. Trailing edge advances cursor in SLOMODE.

PRINT/PLOTCMDDØ — PRINT/PLOT CoMmanD — Initiates a print cycle or, in an incremental plotter, commands plotting of a new channel.

Q6D1 — 2^{6} μs = 64 μs/cycle timing signal.

RCRTXDØ — Reset CRT X-axis sweep — Digital pulse forces CRT display X-axis retrace at FRBLANK time in normal mode or during PREMARK in HORIZ EXPAND mode.

REALSWDØ — REAL time switch — Low when real time display mode is selected.

REALTIMED1 — REAL TIME signal — High when in real time mode.

RESINTD1 — RESet INTegrator — Resets the input card integrator.

RIGHTSWDØ — Cursor RIGHT (→) switch — Normally open side of (cursor) switch. Low when switch is pressed.

RIGHTSWD1 — Cursor RIGHT (→) switch — Normally closed side of (cursor) switch. High when switch is pressed.

SAMPLED1 — SAMPLE command for up/down integrator output — Level at end of SAMPLED1 is held for A/D conversion.

SAMPLEYAN — Plotter SAMPLE and hold Y axis signal — Periodically sampled for PLOT Y during SLOMODE.

SCALE1Ø–1D1 — Full SCALE = 10^{-1} normal — High when SCALE FACTOR 10^4 is selected on front panel and not in LOG mode.

SCALE 1Ø–2D1 — Full SCALE = 10^{-2} normal — High when SCALE FACTOR 10^3 is selected on front panel and not in LOG mode.

SDELAYDØ — Super DELAY — Grounding this line enables external extended-delay option.

SHIFTINDØ — Memory SHIFT command — Shifts data into MOS shift registers from memory counters.

SHIFTOUTDØ — Memory SHIFT command — Shifts data out of MOS shift registers into memory counters.

SIGINAN — Analog Signal Input — Input card signal from preamplifier or test source.

SIGNNORMDØ — Printer SIGN NORMAL mode command — H-P Printer sign will be ± in normal mode (SIGNNORMDØ low) but P or N in peak integrate mode or accumulate cycle mode.

SLOMODED1 — SLOW MODE signal — When PLOT/PRINT switch is pressed, SLOMODE advances cursor at selected rate until channel 499 is reached - activates plotter sweep and output.

SPAREERRORDØ — SPARE ERROR LED input — For option applications requiring an error indication.

SYSRESETDØ — System RESET — Low for ≈1 sec after power on - a spare power-on reset line for initializing options.

TØD1 — Transfer command — Transfers $1Ø^0$ digit (L.S.D.) on all digit-serial busses.

T1D1 — Transfer command — Transfers $1Ø^1$ (10's) digit on all digit-serial busses.

T2D1 — Transfer command — Transfers $1Ø^2$ (100's) digit on all digit-serial busses.

T3D1 — Transfer command — Transfers $1Ø^3$ (1000's) digit on all digit-serial busses.

T4D1 — Transfer command — Transfers $1Ø^4$ (10,000's) digit on all digit-serial busses.

TESTOUT A — Analog TEST signal output — Test switch signal which is positive when Q6D1 is high.

TGATED1 — Time GATE — Pulse whose width is proportional to input signal.

VBLANKD1 — Vidicon BLANK — Turns off vidicon beam when high.

VFRRETRACED1 — Vidicon Frame RETRACE — Retrace command for vidicon frame scan card.

VIDEOTPAN — VIDEO Testpoint — Buffered input card sample and hold output signal. Goes negative when real time display is positive.

VLNDRIVEDØ — Vidicon Line Drive — 64 μs/cycle square wave 90° out of phase with Q6D1. Drives vidicon line scan card.

11.3 SIGNAL ROUTING

SHT 1 OF 7

	FRONT	INPUT	TIMING	MEMORY A	MEMORY B	ARITHMETIC	OUTPUT	DISPLAY DRIVE	CONTROL	PRESET	CURSOR	INTEGRATE	SPARE 1	SPARE 2	NUMERAL BOARD	DIGITAL OUTPUT	REMOTE PROGRAM	BACK PANEL
	1		2	3	4	5	6	7	8	9	10	11	12	13				
1MHZ D1			C						25*		25							
2MHZ D1									24*			24						
4MHZ D1			$\overline{A}$						23*									
8MHZ D1				U	U	17			17*									
16MHZ D1			22						22*									
AØ1 DØ				18,V *		18												
AØ2 DØ				19,W *		19												
AØ4 DØ				20,X *		20												
AØ8 DØ				21,Y *		21												
AACCUMSW DØ	WIRE *		40														50*	
ACCUMCYSW DØ	MBSW *								31							21*		
ACOUNTENA D1			8*	8														
ADR12 B1 BUSS											*		√	√	√	√		
ADR24 D1 BUSS									$\overline{V}$		$\overline{V}$		$\overline{V}$	40,$\overline{V}$	3N12	44		
ADRØ1 D1 BUSS											$\overline{J}$*		$\overline{J}$	30,$\overline{J}$	3N2	15		
ADRØ2 D1 BUSS											$\overline{K}$*		$\overline{K}$	31,$\overline{K}$	3N3	16		
ADRØ4 D1 BUSS											$\overline{L}$*		$\overline{L}$	32,$\overline{L}$	3N4	40		
ADRØ8 D1 BUSS											$\overline{M}$*		$\overline{M}$	33,$\overline{M}$	3N5	41		
ADR11 D1 BUSS											$\overline{N}$*		$\overline{N}$	34,$\overline{N}$	3N6	17		
ADR12 D1 BUSS											$\overline{P}$*	35,$\overline{P}$	35,$\overline{P}$	35,$\overline{P}$	3N7	18		
ADR14 D1 BUSS											$\overline{R}$*		$\overline{R}$	36,$\overline{R}$	3N8	42		
ADR18 D1 BUSS											$\overline{S}$*		$\overline{S}$	37,$\overline{S}$	3N9	43		
ADR21 D1 BUSS											$\overline{T}$*		$\overline{T}$	38,$\overline{T}$	3N10	19		
ADR22D1 BUSS											$\overline{U}$*		$\overline{U}$	39,$\overline{U}$	3N11	20		
ADR24 D1 BUSS									$\overline{V}$		$\overline{V}$*		$\overline{V}$	40,$\overline{V}$	3N12	44		
ADR28 D1 BUSS											$\overline{W}$*		$\overline{W}$	41,$\overline{W}$	3N13	45		
AFULL DØ			29	29*														
ALED DØ	WIRE		$\overline{M}$*															
AMEMERASE DØ			11*	11														
AMEMERSW DØ	MBSW *	35*	35														48*	
ANEG D1				27,$\overline{E}$ *		27												

*designates signal source

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SIGNAL LIST
1205A OMA
SHT 2 OF 7

	FRONT	INPUT 1	TIMING 2	MEMORY A 3	MEMORY B 4	ARITHMETIC 5	OUTPUT 6	DISPLAY DRIVE 7	CONTROL 8	PRESET 9	CURSOR 10	INTEGRATE 11	SPARE 1 12	SPARE 2 13	NUMBRAL BOARD	DIGITAL OUTPUT	REMOTE PROGRAM	BACK PANEL
AOPTHOLD D1			41			14,R *	14					14						
ARITHNEG D1																		
ASTROBE DØ			10*	10														
ASW DØ JPR	MESW *					40										14 *		
AUBUSY D1						J*												
AUCLOCK DØ						F*	F		F			F						
AUSTART DØ JPR/B			27*			H		H			H							
BØ1 DØ					18,V	V												
BØ2 DØ					19,W	W												
BØ4 DØ					20,X *	X												
BØ8 DØ					21,Y *	Y												
BACCUMSW DØ	WIRE *		R														24 *	
BCOUNTENA D1			J*		8													
BFULL DØ			H		29*													
BLED DØ	WIRE		V*															
BMEMERASE DØ			M*		11													
BMEMERSW DØ	MBSW *	36 *	36														49 *	
BNEG D1					27,E *	E												
BOPTHOLD D1			U															
BSTROBE DØ			L*		10													
BSW DØ JPR	MBSW *					41										13 *		
CØ1 D1						10,L *	10					10						
CØ2 D1						11,M *	11					11						
CØ4 D1						12,N *	12					12						
CØ8 D1						13,P *	13					13						
CDOWNCLK D1			17*	17	17													
CHMARK D1		27,E						27	27		27,E *	27						BNC "CURSOR"
CHAN POWER	*ACCYSW *NUHBD																	
COUNTCLOCK D1			K*	9	9													
CRTX (CRTX SHIELD)								U* (17)										BNC "CRTX"
CRTY (CRTY SHIELD)							R* (P)											BNC "CRTY"

*designates signal source

designates possible jumper connection

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SIGNAL LIST
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SHT 3 OF 7

	FRONT	INPUT 1	TIMING 2	MEMORY A 3	MEMORY B 4	ARITHMETIC 5	OUTPUT 6	DISPLAY DRIVE 7	CONTROL 8	PRESET 9	CURSOR 10	INTEGRATE 11	SPARE 1 12	SPARE 2 13	NUMERAL BOARD	DIGITAL OUTPUT	REMOTE PROGRAM	BACK PANEL
CRTZ (CRTZSHIELD)								42* (X) V* (40)										BNC "CRTZ"
CRTZ HIGH (CRTZHISHIELD)																		BNC "CRTZHISHIE
CURSDWN DØ									H*		H	29						
CURSUP DØ									P*		28,F	28						
DAC A+ (DACSHIELD)	MBSW "LOG"						41 (40)											
DACCAL A + (DACCALSHIELD)	LOGSW, WIRE VG POT						38* (37)											
DACEL 1 D1						L*	32											
DACE2 D1						N*	34											
DACE4 D1						J*	30											
DACOUT A+ (DACOUTSHIELD)	WIRE VERT · POT						25* (26)											
DATAREADY D1 J P R									E*							39		
DATAREQ DØ JPR D									-J							22*		
DELBLANK D1			13						N	B,J *								
DELBLANK2 DØ										L							27*	
DELINH D1			R*							R							29	
DELPGM DØ										P							4*	
DIFFSW DØ JPR	M,B,SW "A-B"*															38		
DIG2Ø B1 BUSS												*	√	√	√	√		
DIGØ1 D1 BUSS												H*	H	7,H	1N2	1		
DIGØ2 D1 BUSS												J*	J	8,J	1N3	2		
DIGØ4 D1 BUSS												K*	K	9,K	1N4	26		
DIGØ8 D1 BUSS												L*	L	10,L	1N5	27		
DIG11 D1 BUSS												M*	M	11,M	1N6	3		
DIG12 D1 BUSS												N*	N	12,N	1N7	4		
DIG14 D1 BUSS												P*	P	13,P	1N8	28		
DIG18D1 BUSS												R*	R	14,R	1N9	29		
DIG21 D1 BUSS												S*	S	15,S	1N10	5		
DIG22 D1 BUSS												T*	T	16,T	1N11	6		
DIG24 D1 BUSS												U*	U	17,U	1N12	30		
DIG28 D1 BUSS												V*	V	18,V	1N13	31		

*designates signal source

designates possible jumper connection

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SIGNAL LIST
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SHT 4 OF 7

	FRONT	1 INPUT	2 TIMING	3 MEMORY A	4 MEMORY B	5 ARITHMETIC	6 OUTPUT	7 DISPLAY DRIVE	8 CONTROL	9 PRESET	10 CURSOR	11 INTEGRATE	12 SPARE 1	13 SPARE 2	NUMBRAL BOARD	DIGITAL OUTPUT	REMOTE PROGRAM	BACK PANEL
DIG31 D1												W*	W	19,W	2N1	7		
DIG32 D1												X*	X	20,X	2N2	8		
DIG34 D1												Y*	Y	21,Y	2N3	32		
DIG38 D1												Z*	Z	22,Z	2N4	33		
DIG41 D1 BUSS												$\overline{A}$*	$\overline{A}$	23,$\overline{A}$	2N5	9		
DIG42 D1 BUSS												$\overline{B}$*	$\overline{B}$	24,$\overline{B}$	2N6	10		
DIG44 D1 BUSS												$\overline{C}$*	$\overline{C}$	25,$\overline{C}$	2N7	34		
DIG48 D1 BUSS												$\overline{D}$*	$\overline{D}$	26,$\overline{D}$	2N11	35		
DIGNEG D1												$\overline{E}$*	$\overline{E}$	27,$\overline{E}$	2N10	11		
ENLEDS DØ									$\overline{S}$*						3N1			
ENOR D1									13*			20						
ERRORLED DØ JPR J			16*												2N14			
EXPAND DØ	WIRE HEXP PUT*								9									
FRBLANK D1 JPR C			$\overline{L}$					11,M	11	M	16*						28	
FRRETRACE DØ			14						S		15*						3	
FSHOLDSW DØ	WIRE *		38														25*	
FSLED DØ	WIRE		37*															
HOLD D1 JPR G			39*							6								
HOREX A-	WIRE H. EXPUT *							V										
INBLANK D1			12								17*							
INT D1									$\overline{N}$			33*						
INTERROR DØ JPR A			21									32*						
INTSW DØ	MRSW "Σ"*											34				12		COM. .28 x10-x28 SWDS
INTX1ØSW DØ JPR												E			1N14	37*		B.P.C.D INTx10 x100
INTX1ØØSW DØ															1N1			
LEFTSW DØ	MBSW*								$\overline{A}$									
LEFTSW D1	MBSW*								Z									
LNADVCLK DØ									$\overline{E}$							23*		
LNSTROBE DØ												42					13*	
LNZERO DØ	MBSW*	30*										29				49*		
LOG D1						$\overline{P}$*	35											
LOGSW DØ	MBSW* WIRE FSSW					42										24		
MRESET DØ JPR F			26*						H									
OPTBLANK DØ			42															

*designates signal source ▮ designates possible jumper connection

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SIGNAL LIST
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SHT 5 OF 7

	FRONT	INPUT 1	TIMING 2	MEMORY A 3	MEMORY B 4	ARITHMETIC 5	OUTPUT 6	DISPLAY DRIVE 7	CONTROL 8	RESET 9	CURSOR 10	INTEGRATE 11	SPARE 1 12	SPARE 2 13	NUMERAL BOARD	DIGITAL OUTPUT	REMOTE PROGRAM	BACK PANEL
ORTØ									12			15*						
ORT2 DØ									7			16*						
ORT4 DØ									26			26*						
PGMDEL4 B1 BUSS										√							*	
PGMDELØ1 D1 BUSS										$\overline{D}$							7*	
PGMDELØ2 D1 BUSS										$\overline{C}$							31*	
PGMDELØ4 D1 BUSS										$\overline{B}$							6*	
PGMDELØ8 D1 BUSS										$\overline{A}$							30*	
PGMLN12 B1 BUSS											√						*	
PGMLNØ1 D1 BUSS											32						10*	
PGMLNØ2 D1 BUSS											33						35*	
PGMLNØ4 D1 BUSS											31						34	
PGMLNØ8 D1											30						9	
PGMLN11 D1 BUSS											36						12*	
PGMLN12 D1 BUSS											37						37*	
PGMLN14 D1 BUSS											35						36*	
PGMLN18 D1 BUSS											34						11*	
PGMLN21 D1 BUSS											38						15*	
PGMLN22 D1 BUSS											40						14*	
PGMLN24 D1 BUSS											39						39*	
PGMLN28 D1 BUSS											41						33*	
PGMPRE16 B1 BUSS										√							*	
PGMPREØ1 D1 BUSS										$\overline{J}$							22*	
PGMPREØ2 D1 BUSS										$\overline{H}$							33*	
PGMPREØ4 D1 BUSS										$\overline{F}$							3*	
PGMPREØ8 D1 BUSS										$\overline{E}$							32*	
PGMPRE11 D1										$\overline{N}$							42*	
PGMPRE12 D1										$\overline{M}$							17*	
PGMPRE14 D1										$\overline{L}$							41*	
PGMPRE18 D1										$\overline{K}$							16*	

*designates signal source

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SIGNAL LIST
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	FRONT	INPUT 1	TIMING 2	MEMORY A 3	MEMORY B 4	ARITHMETIC 5	OUTPUT 6	DISPLAY DRIVE 7	CONTROL 8	PRESET 9	CURSOR 10	INTEGRATE 11	SPARE 1 12	SPARE 2 13	NUMERAL BOARD	DIGITAL OUTPUT	REMOTE PROGRAM	BACK PANEL
PGMPRE21 D1 BUSS										$\overline{T}$							20*	
PGMPRE22 D1 BUSS										$\overline{S}$							45*	
PGMPRE24 D1 BUSS										$\overline{R}$							21*	
PGMPRE28 D1 BUSS										$\overline{P}$							46*	
PGMPRE31 D1 BUSS										$\overline{X}$							18*	
PGMPRE32 D1 BUSS										$\overline{W}$							43*	
PGMPRE34 D1 BUSS										$\overline{V}$							19*	
PGMPRE38 D1 BUSS										$\overline{U}$							44*	
PLOTCMD DØ									14*							48		
PLOTNULL D1									W							47*		
PLOTSWØ1 D1									41									RATE SW
PLOTSWØ2 D1									42									RATE SW
PLOTSWØ4 D1									40									RATE SW
PLOTSWØ8 D1									39									RATE SW
PLOTX (PLOTXSHIELD)								26 (D)*										BNC PLOTX
PLOTY (PLOTYSHIELD)								K* (9)										ENC PLOTY
P/PSW DØ	MBSW *							43	43							46*		
PRECLOCK2 DØ										K							2*	
PRECOMP D1			W							19*								
PREHOLDSW DØ JPR E	WIRE *		$\overline{W}$						6								23*	
PRELED DØ	WIRE		$\overline{X}$*															
PREMARK D1 JPR									8		24*							
PREPGM DØ										20							5*	
PRERESET DØ									5*	5								
PRINTCMD DØ									14*							48		
PRINTINH DØ									W							47*		
PRINT/PLOTCMD DØ									14*							48		
Q6 D1		8	6*															
RCRTX DØ								10,L	10*									
REALSW DØ	MBSW *		25			39			38								47*	
REALTIME D1			P*						P									
RESINT D1		7	5*															
RIGHTSW DØ	MBSW *								$\overline{C}$									

*designates signal source ■ designates possible jumper connection

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SIGNAL LIST
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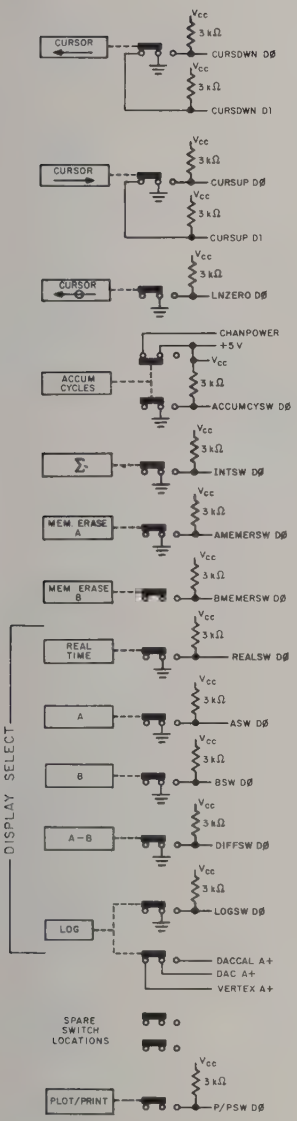
SHT 7 OF 7

	FRONT	INPUT 1	TIMING 2	MEMORY A 3	MEMORY B 4	ARITHMETIC 5	OUTPUT 6	DISPLAY DRIVE 7	CONTROL 8	PRESET 9	CURSOR 10	INTEGRATE 11	SPARE 1 12	SPARE 2 13	NUMERAL BOARD	DIGITAL OUTPUT	REMOTE PROGRAM	BACK PANEL
RIGHTSW D1	MBSW*								B									
SAMPLE D1		9	7															
SAMPLEY AN							E*	E										
SCALE10-1 D1	WIRE PSSW*					K												
SCALE10-2 D1	WIRE PSSW*					M												
SDELAY DØ JPR H										7,H							40*	
SHIFTIN DØ			F*	6	6													
SHIFTOUT DØ			H*	7	7				7									
SIGIN AN (SIGINSHIELD)	COAX* SAIEW	10 (11)																
SIGNNORM DØ									M*							36		
SLOMODE D1								29	29*									
SPAREERROR DØ			20 PAD															
SYSRESET DØ		34*																
TØ D1				12,N	12,N	5*	5					5						
T1 D1				13,P	13,P	6*	6					6						
T2 D1				14,R	14,R	7*	7					7						
T3 D1				15,S	15,S	8*	8					8						
T4 D1				16,T	16,T	9*	9					9						
TESTOUT A+ (TESTOUTSHIELD)	COAX* SHIELD	5* (6)																
TGATE D1		19*	19															
VBLANK D1	WIRE		43*															
VFRRETRACE D1	WIRE		15															
VIDEOTP AN (VIDGOTPSHIELD)		15* (14)																BNC "VIDEO
VLNDRIVE DØ	WIRE TO LINE-SCAN		E*															
VERTEX A+	WIRE* VEX POTSC LOGSW																	
+15V		4	4	4	4	4	4	4	4	4	4	4	4	4				
-15V	√	D	D	D	D	D	D	D	D	D	D	D	D	D				
+5V	√	2,B	2,B	2,B	2,B	2,B	2,B	2,B	2,B	2,B	2,B	2,B	2,B	2,B				
+5 BIAS1 JPR																25		
+5 BIAS2 JPR																	1	
GROUND	√	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	1,A,$\bar{Y}$	√	50	26	

*designates signal source

designates possible jumper connection

11.4 FRONT-PANEL SWITCH CONNECTIONS



11.5 MAIN FRAME SCHEMATIC HARNESS ASSEMBLY

LEFT TO RIGHT SEQUENCE AT MOTHER BOARD	WIRE CONNECTS FROM MOTHER BOARD TO:	WIRE COLOR	SIGNAL AND FLOW DIRECTION
1	F. PANEL	BLACK	← GROUND
2	LED BD.	RED	← +5V
3	F. PANEL	BROWN	← -15V
20[2]	NUM. BD	WHITE	← CHAN POWER[2]
4	SYS. PWR.	WH/GRA	← VLNDRIVE DØ
32[2]	SYS. PWR	RED	→ +5V[2]
5	IN SW BD	RG174	← TESTOUT A+
5s		SHIELD	(TESTOUTSHIELD)
6	IN SW BD	RG174	→ SIGIN AN
6s		SHIELD	(SIGINSHIELD)
7s	B.P. BNC	SHIELD	← (VIDEOTPSHIELD)
7		RG174	VIDEOTP AN
8	SYS. PWR	ORANGE	← VFRRETRACE D1
9	F. PANEL	YELLOW	→ EXPAND DØ
10	F. PANEL	GREEN	→ HOREX A-
11	F. PANEL	RG174	← DACOUT A+
11s		SHIELD	(DACOUTSHIELD)
12	F. PANEL	BLUE	→ SCALE 1Ø -1 DØ
13	F. PANEL	VIOLET	→ SCALE 1Ø-2 DØ
14	LED BD.	GRAY	← ALED DØ
15	IN SW BD	WHITE	→ BACCUMSW DØ
16	LED BD	WH/BLK	← FSLED DØ
17	IN SW BD	WH/BRN	→ FSHOLDSW DØ
18	IN SW BD	WH/RED	→ AACCUMSW DØ
19	LED BD	WH/ORN	← BLED DØ
20	IN SW BD	WH/YEL	→ PREHOLDSW DØ
21	LED BD	WH/GRN	← PRELED DØ
22	SYS. PWR	WH/BLU	← V BLANK D1
23	F. PANEL	WH/V10	← LOG SW DØ
24s	F. PANEL	SHIELD	→ (DACCALSHIELD)
24		RG174	DACCAL A+
25s	F. PANEL	SHIELD	→ (VERTEXSHIELD)
25		RG174	VERTEX

1 ← INDICATES SIGNAL HAS ORIGIN AT MOTHER BOARD;
→ INDICATES SIGNAL GOES TO MOTHER BOARD
2 CHANNEL POWER (20) AND SYSTEM POWER (32; +5V) NOT IN SEQUENCE.

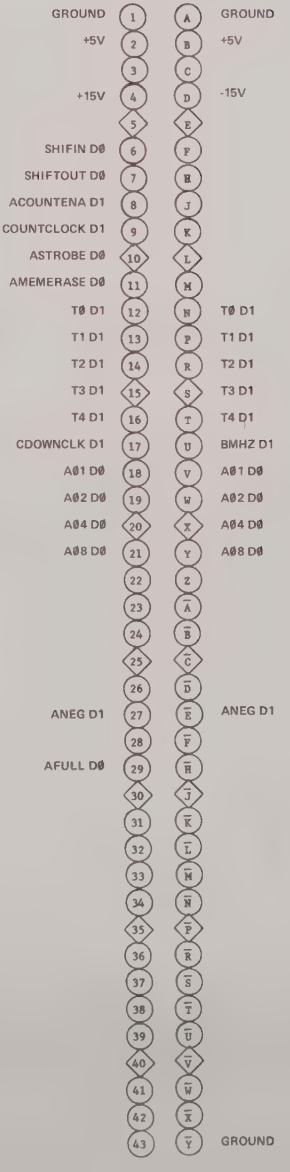
11.6 INTERNAL CONNECTOR PIN ASSIGNMENTS

① INPUT

② TIMING

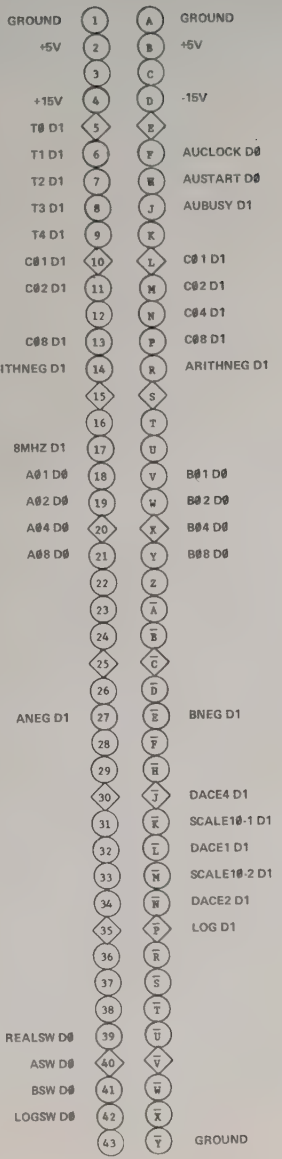
GROUND 1 A GROUND
+5V 2 B +5V
3 C
+15V 4 D -15V
RESINT D1 5 E VLNDRIVE D0
Q6 D1 6 F SHIFTIN D0
SAMPLE D1 7 H SHIFTOUT D0
ACOUNTENA D1 8 J BCOUNTENA D1
9 K COUNTCLOCK D1
ASTROBE D0 10 L BSTROBE D0
AMEMERASE D0 11 M BMEMERASE D0
INBLANK D1 12 N
DELBLANK D1 13 P REALTIME D1
FRRETRACE D0 14 R DELINH D1
VFRETRACE D1 15 S
ERRORLED D0 16 T
CDOWNCLK D1 17 U
18 V
TGATE D1 19 W PRECOMP D1
SPAREERROR D0 20 X
INTERROR D0 21 Y
16MHZ D1 22 Z
23 A 4MHZ D1
24 B
REALSW D0 25 C 1MHZ D1
MRESET D0 26 D
AUSTART D0 27 E
28 F
AFULL D0 29 H BFUL D0
30 J
31 K
32 L FRBLANK D1
33 M ALED D0
34 N
AMEMERSW D0 35 P
BMEMERSW D0 36 R BACCUMSW D0
FSLED D0 37 S
FSHOLDSW D0 38 T
HOLD D1 39 U BOPTHOLD D1
AACCUMSW D0 40 V BLED D0
AOPTHOLD D1 41 W PREHOLDSW D0
OPTBLANK D0 42 X PRELED D0
VBLANK D1 43 Y GROUND

③ MEMORY A

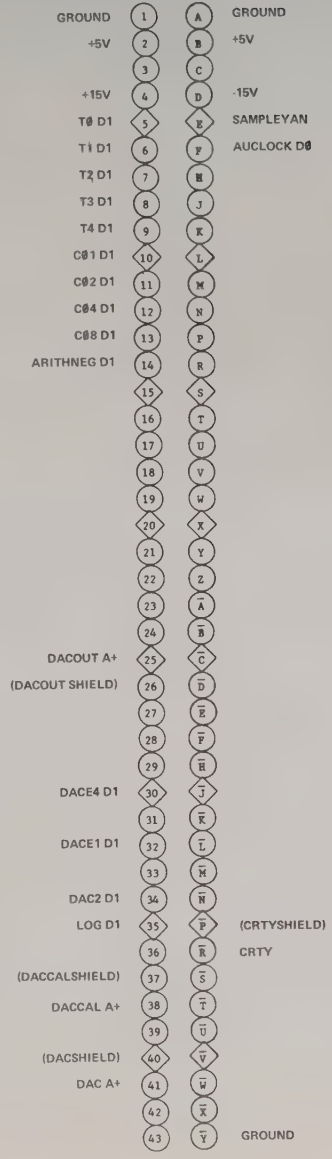


④ MEMORY B

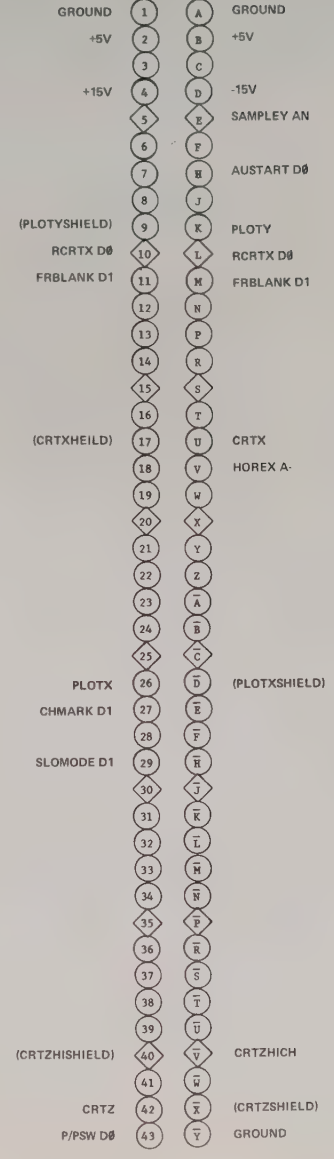
5 ARITHMETIC



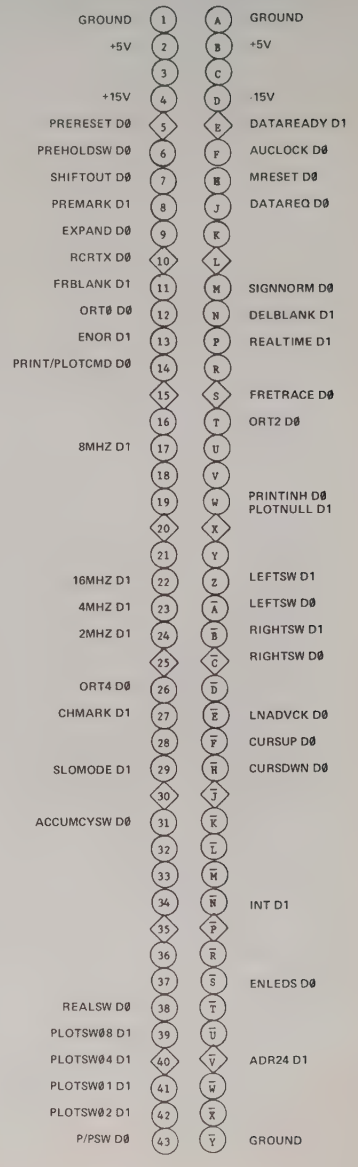
6 OUTPUT



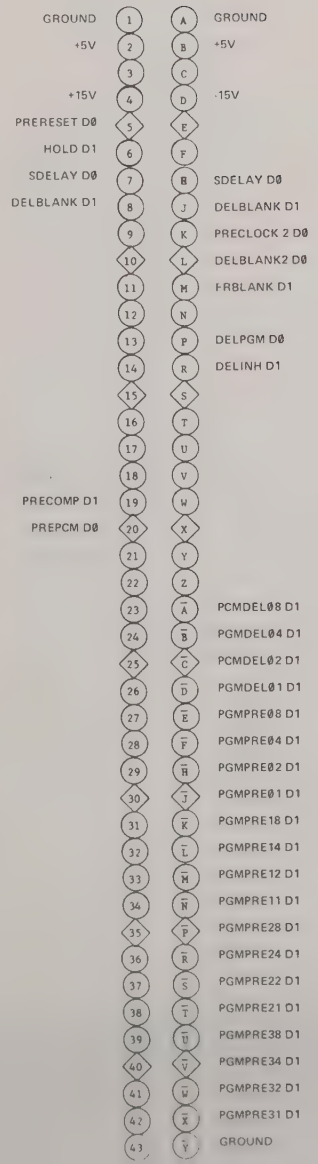
7 DISPLAY DRIVE



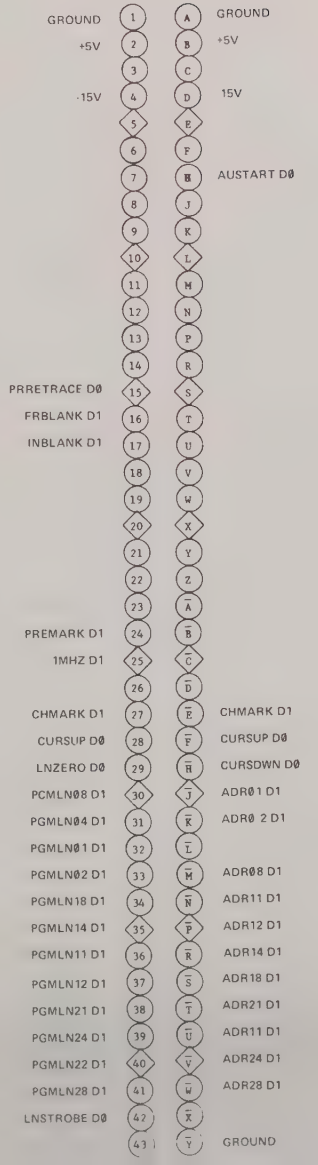
8 CONTROL


GROUND 1 A GROUND
+5V 2 B +5V
3 C
+15V 4 D -15V
PRERESET D0 5 E DATAREADY D1
PREHOLDSW D0 6 F AUCLOCK D0
SHIFTOUT D0 7 H MRESET D0
PREMARK D1 8 J DATAREQ D0
EXPAND D0 9 K
RCRTX D0 10 L
FRBLANK D1 11 M SIGNNORM D0
ORT0 D0 12 N DELBLANK D1
ENOR D1 13 P REALTIME D1
PRINT/PLOTCMD D0 14 R
15 S FRETRACE D0
16 T ORT2 D0
8MHZ D1 17 U
18 V
19 W PRINTINH D0
PLOTNULL D1
20 X
21 Y
16MHZ D1 22 Z LEFTSW D1
4MHZ D1 23 A LEFTSW D0
2MHZ D1 24 B RIGHTSW D1
25 C RIGHTSW D0
ORT4 D0 26 D
CHMARK D1 27 E LNADVCK D0
28 F CURSUP D0
SLOMODE D1 29 H CURSDWN D0
30 J
ACCUMCYSW D0 31 K
32 L
33 M
34 N INT D1
35 P
36 R
37 S ENLEDS D0
REALSW D0 38 T
PLOTSW08 D1 39 U
PLOTSW04 D1 40 V ADR24 D1
PLOTSW01 D1 41 W
PLOTSW02 D1 42 X
P/PSW D0 43 Y GROUND

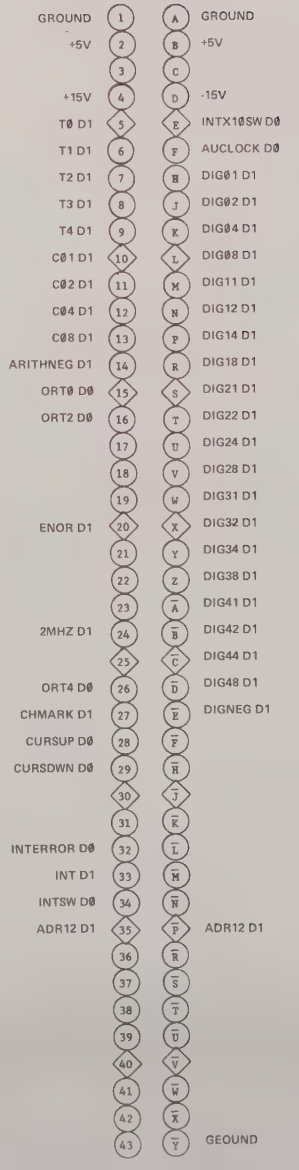
9 PRESET



10 CURSOR



11 INTEGRATE


GROUND 1 A GROUND
+5V 2 B +5V
3 C
+15V 4 D -15V
T0 D1 5 E INTX10SW D0
T1 D1 6 F AUCLOCK D0
T2 D1 7 H DIG01 D1
T3 D1 8 J DIG02 D1
T4 D1 9 K DIG04 D1
C01 D1 10 L DIG08 D1
C02 D1 11 M DIG11 D1
C04 D1 12 N DIG12 D1
C08 D1 13 P DIG14 D1
ARITHNEG D1 14 R DIG18 D1
ORT0 D0 15 S DIG21 D1
ORT2 D0 16 T DIG22 D1
17 U DIG24 D1
18 V DIG28 D1
19 W DIG31 D1
ENOR D1 20 X DIG32 D1
21 Y DIG34 D1
22 Z DIG38 D1
23 A DIG41 D1
2MHZ D1 24 B DIG42 D1
25 C DIG44 D1
ORT4 D0 26 D DIG48 D1
CHMARK D1 27 E DIGNEG D1
CURSUP D0 28 F
CURSDWN D0 29 H
30 J
31 K
INTERROR D0 32 L
INT D1 33 M
INTSW D0 34 N
ADR12 D1 35 P ADR12 D1
36 R
37 S
38 T
39 U
40 V
41 W
42 X
43 Y GEOUND

12 SPARE 1

(13) SPARE 2

GROUND	1	A	GROUND
+5V	2	B	+5V
	3	C	
+15V	4	D	15V
	5	E	
	6	F	
DIG01 D1	7	H	DIG01 D1
DIG02 D1	8	J	DIG02 D1
DIG04 D1	9	K	DIG04 D1
DIG08 D1	10	L	DIG08 D1
DIG11 D1	11	M	DIG11 D1
DIG12 D1	12	N	DIG12 D1
DIG14 D1	13	P	DIG14 D1
DIG18 D1	14	R	DIG18 D1
DIG21 D1	15	S	DIG21 D1
DIG22 D1	16	T	DIG22 D1
DIG24 D1	17	U	DIG24 D1
DIG28 D1	18	V	DIG28 D1
DIG31 D1	19	W	DIG31 D1
DIG32 D1	20	X	DIG32 D1
DIG34 D1	21	Y	DIG34 D1
DIG38 D1	22	Z	DIG38 D1
DIG41 D1	23	A	DIG41 D1
DIG42 D1	24	B	DIG42 D1
DIG44 D1	25	C	DIG44 D1
DIG48 D1	26	D	DIG48 D1
DIGNEG D1	27	E	DIGNEG D1
	28	F	
	29	H	
ADR01 D1	30	J	ADR01 D1
ADR02 D1	31	K	ADR02 D1
ADR04 D1	32	L	ADR04 D1
ADR08 D1	33	M	ADR08 D1
ADR11 D1	34	N	ADR11 D1
ADR12 D1	35	P	ADR12 D1
ADR14 D1	36	R	ADR14 D1
ADR18 D1	37	S	ADR18 D1
ADR 21 D1	38	T	ADR21 D1
ADR22 D1	39	U	ADR22 D1
ADR24 D1	40	V	ADR24 D1
ADR28 D1	41	W	ADR28 D1
	42	X	
	43	Y	GROUND

11.7 PIN ASSIGNMENTS FOR MOTHER-BOARD CABLE CONNECTORS

1N

INTX100SW D0	1	14	INTX10SW D0
DIG01 D1	2	13	DIG28 D1
DIG02 D1	3	12	DIG24 D1
DIG04 D1	4	11	DIG22 D1
DIG08 D1	5	10	DIG21 D1
DIG11 D1	6	9	DIG18 D1
DIG12 D1	7	8	DIG14 D1

2N

DIG31 D1	1	14	ERRORLED D0
DIG32 D1	2	13	
DIG34 D1	3	12	
DIG38 D1	4	11	DIG48 D1
DIG41 D1	5	10	DIGNEG D0
DIG42 D1	6	9	
DIG44 D1	7	8	

3N

ENLEDS D0	1	14	
ADR01 D1	2	13	ADR28 D1
ADR02 D1	3	12	ADR24 D1
ADR04 D1	4	11	ADR22 D1
ADR08 D1	5	10	ADR21 D1
ADR11 D1	6	9	ADR18 D1
ADR12 D1	7	8	ADR14 D1

11.8 INTERFACE CONNECTOR PIN ASSIGNMENTS

TTL DIGITAL OUTPUT

DIG01 D1	1	26	DIG04 D1
DIG02 D1	2	27	DIG08 D1
DIG11 D1	3	28	DIG14 D1
DIG12 D1	4	29	DIG18 D1
DIG21 D1	5	30	DIG24 D1
DIG22 D1	6	31	DIG28 D1
DIG31 D1	7	32	DIG34 D1
DIG32 D1	8	33	DIG38 D1
DIG41 D1	9	34	DIG44 D1
DIG42 D1	10	35	DIG48 D1
DIGNEG D1	11	36	SIGNNORM D0
INTSW D0	12	37	INTX10SW D0
BSW D0	13	38	DIFFSW D0
ASW D0	14	39	DATAREADY D1
ADR01 D1	15	40	ADR04 D1
ADR02 D1	16	41	ADR08 D1
ADR11 D1	17	42	ADR14 D1
ADR12 D1	18	43	ADR18 D1
ADR21 D1	19	44	ADR24 D1
ADR22 D1	20	45	ADR28 D1
ACCUMCYSW D0	21	46	P/PSW D0
DATAREQ D0	22	47	PRINTINH D0
LNADVCLK D0	23	48	PRINTCMD D0
LOGSW D0	24	49	LNZERO D0
+5BIAS1	25	50	GROUND

TTL REMOTE PROGRAM

+5BIAS2	1	26	GROUND
PRECLOCK2 D0	2	27	DELBLANK2 D0
FRRETRACE D0	3	28	FRBLANK D1
DELPGM D0	4	29	DELINH D1
PREPGM D0	5	30	PGMDEL08 D1
PGMDEL04 D1	6	31	PGMDEL02 D1
PGMDEL01 D1	7	32	PGMPRE08 D1
PGMPRE04 D1	8	33	PGMPRE02 D1
PGMLN08 D1	9	34	PGMLN04 D1
PGMLN01 D1	10	35	PGMLN02 D1
PGMLN18 D1	11	36	PGMLN14 D1
PGMLN11 D1	12	37	PGMLN12 D1
LNSTROBE D0	13	38	PGMLN28 D1
PGMLN22 D1	14	39	PGMLN24 D1
PGMLN21 D1	15	40	SDELAY D0
PGMPRE18 D1	16	41	PGMPRE14 D1
PGMPRE12 D1	17	42	PGMPRE11 D1
PGMPRE31 D1	18	43	PGMPRE32 D1
PGMPRE34 D1	19	44	PGMPRE38 D1
PGMPRE21 D1	20	45	PGMPRE22 D1
PGMPRE24 D1	21	46	PGMPRE28 D1
PGMPRE01 D1	22	47	REALSW D0
PREHOLDSW D0	23	48	AMEMERSW D0
BACCUMSW D0	24	49	BMEMERSW D0
FSHOLDSW D0	25	50	AACCUMSW D0

SECTION XII
TIMING DIAGRAMS AND SCHEMATICS

12.1 DISCUSSION OF TIMING DIAGRAMS

The six TIMING DIAGRAMS show successively finer details of the O.M.A. system timing.

12.1A DIAGRAM #1 (Figure XII-1)

This diagram shows the system timing for a typical measurement with a PRESET HOLD at PRESET = 2, and a spectral input such as the mercury lines from a fluorescent lamp. This drawing also shows the frame-cycle timing for the several cycles involved in such a measurement. Note that the frame retrace and frame blank times (FRRETRACED$\emptyset$ and FRBLANKD1) are 6 and 12 channel times out of the 512 channel times in a cycle. The width of these two pulses, and the time delay between PREMARKD1 and CHMARKD1 have been exaggerated to clearly indicate the timing functions in the frame cycle.

12.1B DIAGRAM #2 (Figure XII-2)

This diagram shows the input signal processing of several channels within one frame cycle. The effect of the TEST input mode is shown, as well as the typical signal characteristics associated with the small signal region including the signal peak, indicated on timing diagram #1.

12.1C DIAGRAM #3 (Figure XII-3)

This diagram shows the rest of the signal process as the several channels of data indicated on timing diagrams #1 and #2 are converted into digital form and processed through the memory into digital and CRT outputs. Note that as one channel is being displayed at the CRT, the next channel is undergoing A/D conversion on the INPUT and TIMING cards and in the counter stage of the MEMORY card, while the channel after that is being scanned at the vidicon and passed to the up-down integrator portion of the analog dark current subtraction process. The two "analog" appearing graphs in the middle of this diagram do not represent actual signals in the system. These are the graphic representation of the status of the 21-bit, 8 BCD digit and sign digital-counter stage of the MEMORY card as the same 5 channels of data are processed during the first and second frame cycles of the measurement shown in timing diagram #1. On the other hand, the CRT Y and CRT Z signals at the bottom of the diagram show the actual signals and analog output voltages with the system adjusted for use with the Tektronix 604 display. Note that the five pulses on the ENORD1 (Enable Output Register) line occur only once during each 32.768 ms frame cycle and transfer only the cursor selected channel to the output register on the INTEGRATE card.

12.1D DIAGRAM #4 (Figure XII-4)

This diagram shows the details of the signal control and transfer logic for a single 64 μs channel time. The timing relationships shown assume ideal logic. However, there is typically 10 ns propagation delay between successive stages of the timing chain. Thus, as indicated at the right edge of this drawing, the falling edge of Q1D1 occurs about 10 nS after a falling edge of 1MHZS1, and the falling edge of Q2D1 is 10 nS after a falling edge of Q1D1 and so on. A falling edge of Q6D1 will typically be 60 - 100 ns after the corresponding transition of 1MHZD1.

12.1E DIAGRAM #5 (Figure XII-5)

(1) Timing diagram #5a shows the fine details of the 6.25 μs arithmetic cycle portion of each channel cycle. The propagation delay situation mentioned previously will cause these signals to vary noticeably from the timing relationships shown. However, the arithmetic output data on the C$\emptyset$4B1 buss will always be stable during the intervals during which AUCLOCKD$\emptyset$ is low. These intervals are the MIDDIGIT and CYCLE2 times mentioned in the logic description in the manual.

(2) Timing diagram #5b shows the details of the memory-register channel shift timing. Key features include:

(a) The 400 ns to 600 ns pulse width of MOS clocks 0_{in} and 0_{out} are controlled by capacitors C1 and C2 on each MEMORY card. If this pulse width is less than 400 ns, there may be a failure mode in which the sign bit of some channels is lost when switching from DISPLAY SELECT "A" to REAL TIME and back, while both memory and real time have positive and negative channel magnitudes. This causes memory values such as −20 to appear as their complement, e.g., +99980. The correct value for C1 and C2 is .0018 μF.

(b) The MEMORY A signal ASTROBED$\emptyset$ is modified in the REAL TIME mode to reload the old shift register output into the counting register just before the shift register input is clocked by the rising edge of 0_{in}. This saves the "A MEMORY" contents while the counter is used for real time A/D conversion. In effect, it counteracts the effect of the AMEMERASED$\emptyset$, CDWNCLKD1, and COUNTCLOCKD1 signals.

(c) The AMEMERASED$\emptyset$ pulse that clears the counter at the beginning of the REAL TIME channel cycle.

(d) The "A" or "B" MEMORY ERASE function turns on the corresponding AMEMERASED$\emptyset$ or BMEMERASED$\emptyset$ pulse as shown, either for all 512 channel times of a 32.768 ms frame cycle, or for none of the channel times of a frame cycle. Thus, there can be no partial or incomplete memory erasures. The erase pulses clear the counters, which causes a "zero" to be loaded into the shift registers by 0_{in}, 62.5 μs later.

12.1F DIAGRAM #6 (Figure XII-6)

(1) Timing diagram #6a is a detail of the frame blank retrace interval timing. The important details of this drawing are:

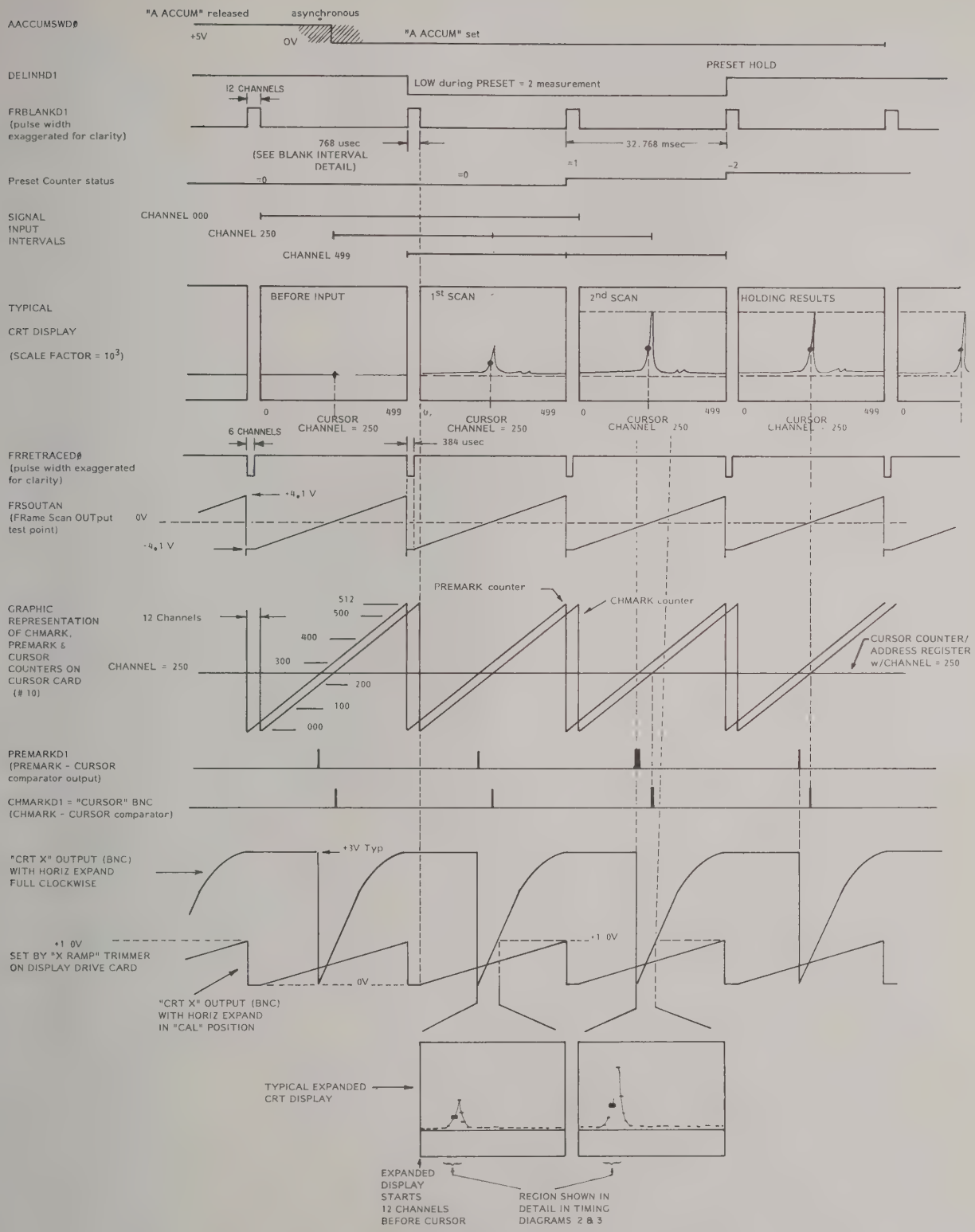
(a) There are scanned bu unused channels at each end of the vidicon detector scan pattern. These are channels "500" and "501" after channel 499, and channels "508" through "511" after the retrace is completed, and before channel 000. These extra scan lines allow channels 000 and 499 to be free of the nonuniformities which occur in the edge of the target scan, due to the lateral charge effects.

(b) Because the channel output time is almost two channel times after the scan (see timing diagram #3), several different blanking signals are required. FRBLANKD1 is the output for the CRT display blanking interval. INBLANKD1 is used in the TIMING card to turn off the COUNTCLOCKD1 pulses associated with the unused scan channels so that the FULL SCALE HOLD and INPUT LIMIT LED circuits will not be activated by the edge effects on these channels.

(c) During the FRRETRACEDØ portion of the INBLANKD1 interval, a single four-microsecond pulse is gated onto the COUNTCLOCKD1 line during each channel time. This is the 4 μs RESINTD1 interval indicated on timing diagram #4. When the memory counter is activated by an ACCUM operation, these pulses provide the one count per-frame-scan function for the ACCUM CYCLES readout. When the ACCUM CYCLES mode is selected, a circuit on the CONTROL card causes the ENORD1 function to be triggered by the trailing edge of FRRETRACEDØ instead of the CHMARKD1 signal. Since the FREETRACEDØ signal is turned on and off by an AUSTARTDØ pulse, the last of the ACCUM CYCLES channels (#506) will be transferred into the digital output register (on the INTEGRATE card) instead of the cursor-selected channel data.

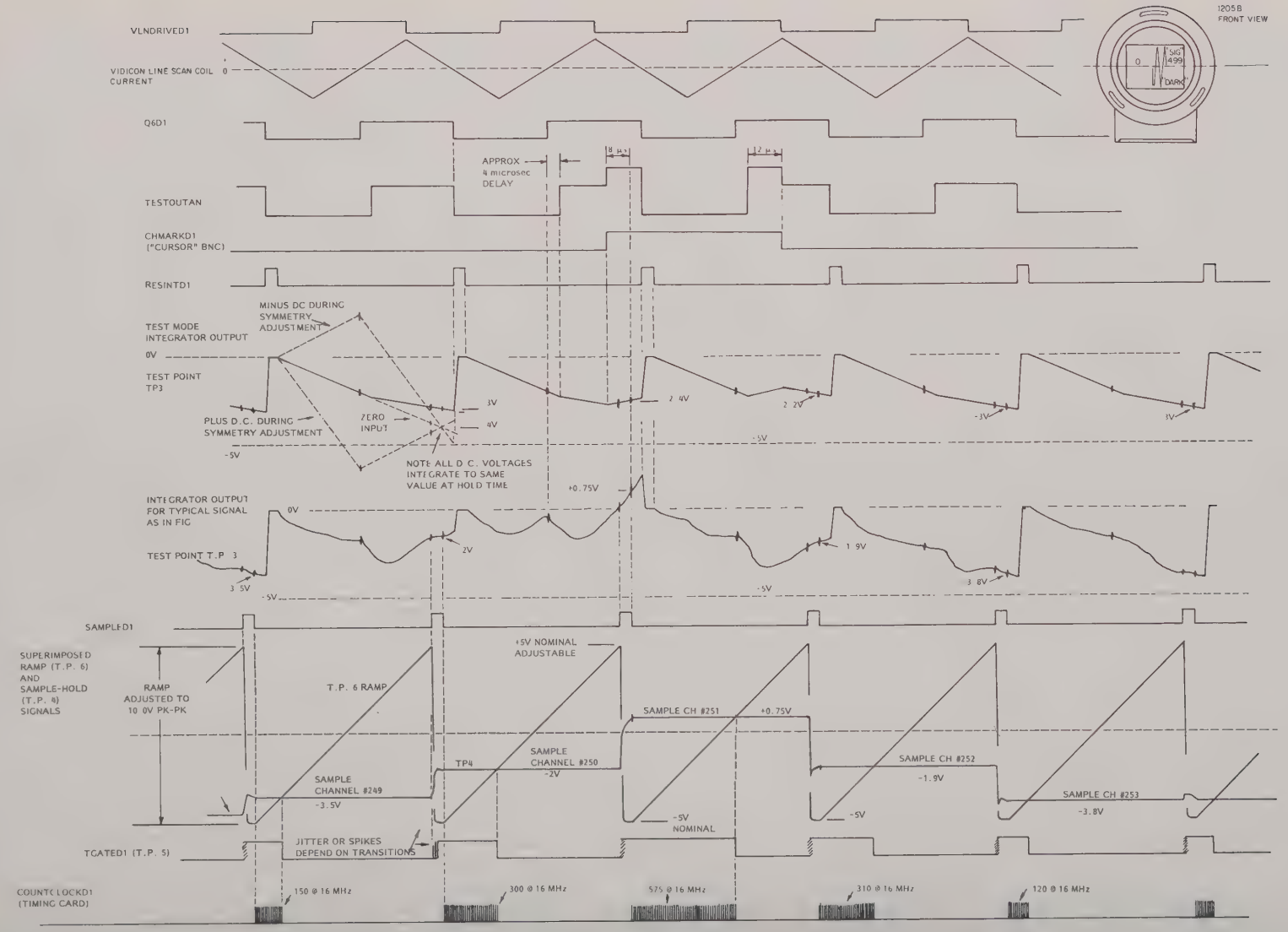
(2) Timing diagram #6b shows the signal characteristics for the counter integrated circuits (ICs) in the system. Most of the MSI function blocks in the circuit diagrams are one of the counter types identified on this drawing. These counters are of two basic types: one-way, up-counting ripple counters; and synchronous up/down counters. Each type includes both binary and Binary Coded Decimal (BCD) types which, except for the counting modulus, are pin-for-pin compatible. Within each of the four subgroups are several part numbers representing different manufacturers and ICs with identical function but different speed/power/fanout tradeoffs. For repair purposes, a low-power IC may be replaced with a higher-speed, higher power part of identical function, but a low power IC must *never* be used to replace a higher speed/fanout unit unless the low power IC is called out on the schematic. 74 LS--ICs, if available, are slightly preferable to the corresponding AM 93L--item. A replacement table for equivalent IC types which have been interchanged during the production history of the 1205A is provided below.

IC Type, Early Runs	Equiv. IC, Later Runs
8881	7401
8890	7404
8293	8281
8292	8280
8815	7425
8551	74173
8H80	74H00



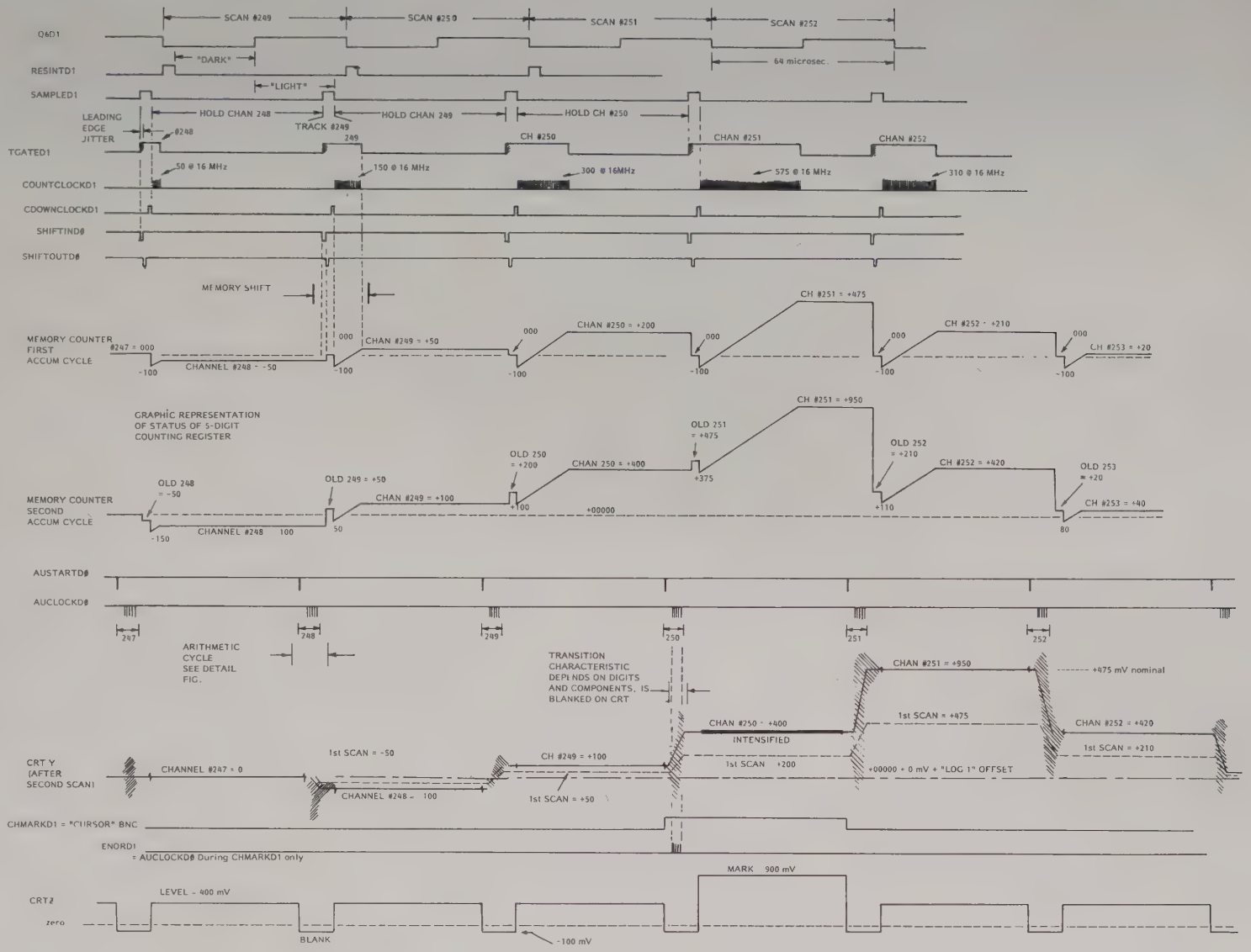
TIMING DIAGRAM #1

Figure XII-1. SYSTEM TIMING, MEASUREMENT CYCLE, AND FRAME CYCLE



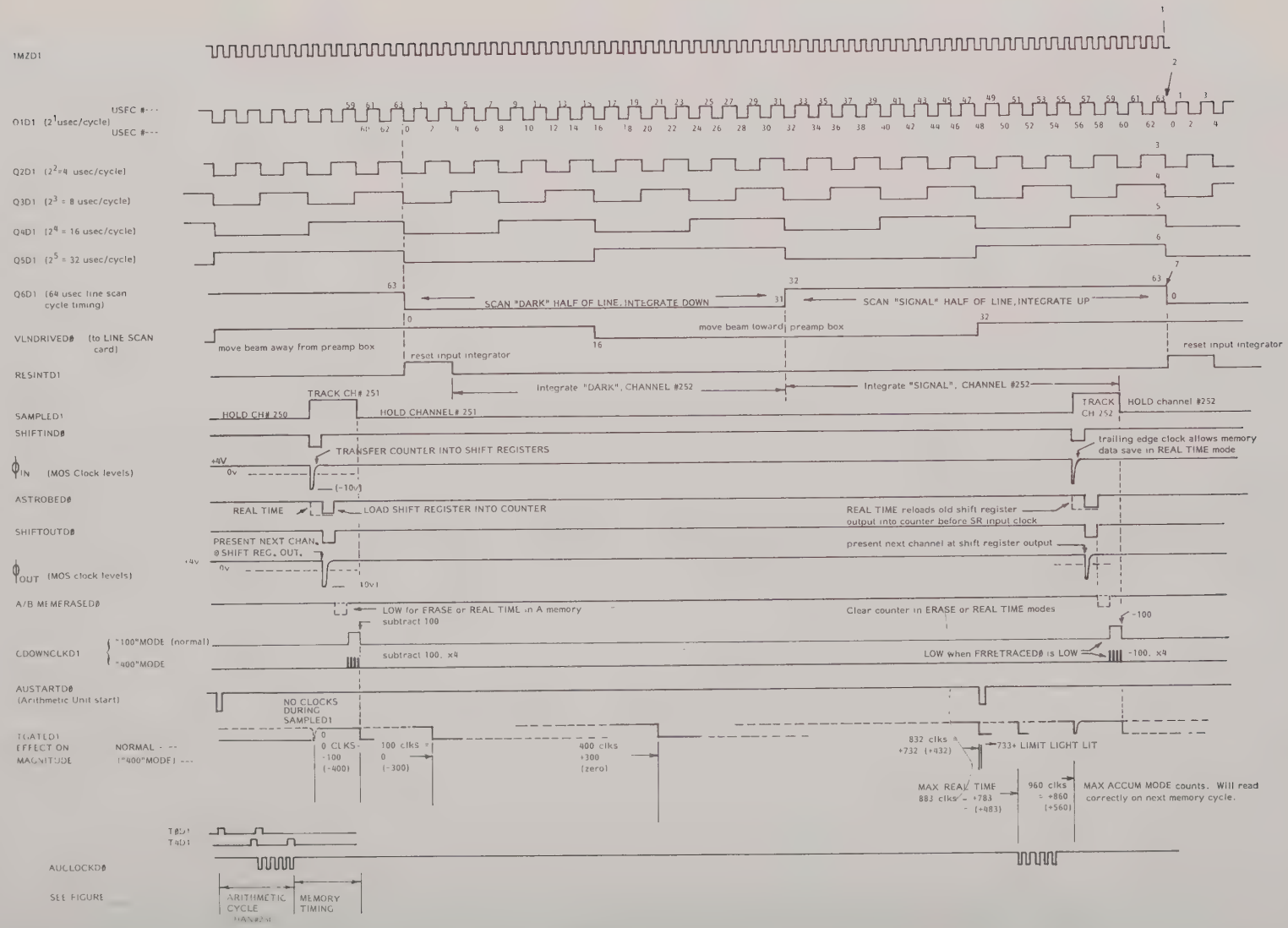
TIMING DIAGRAM #2

Figure XII-2. VIDICON SCAN AND A-D CONVERSION FOR SEVERAL 64 μSEC CHANNEL TIMES



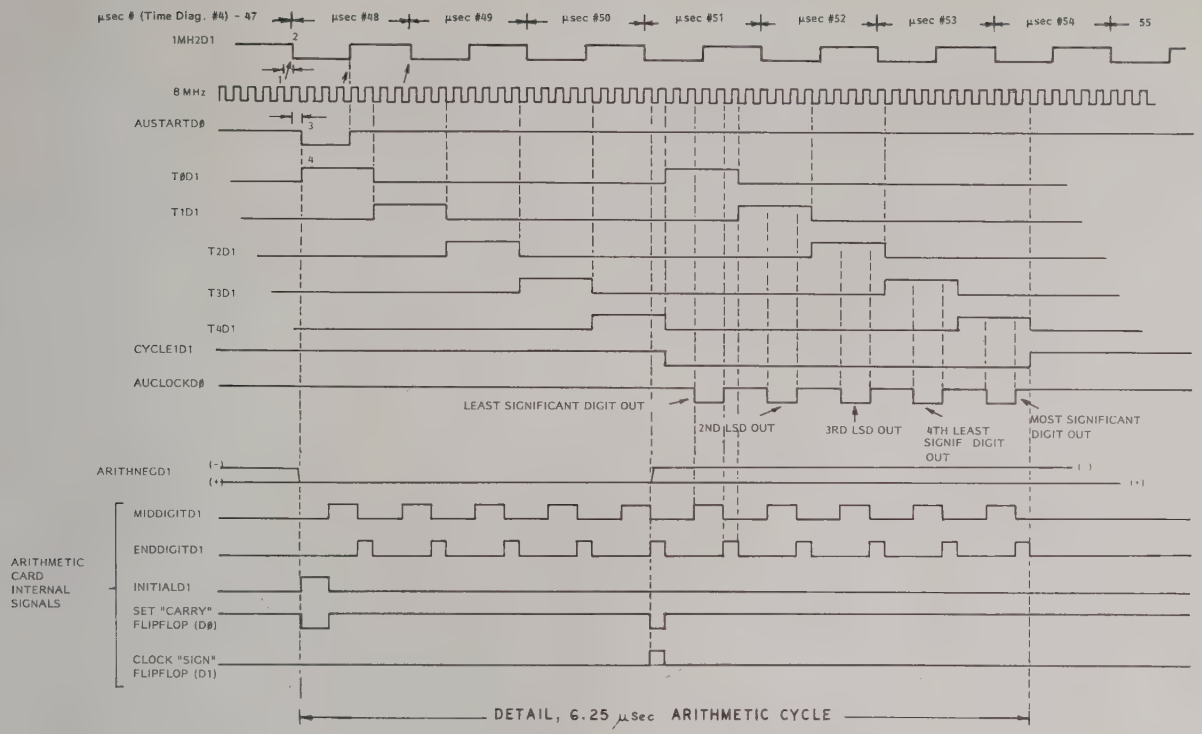
TIMING DIAGRAM #3

Figure XII-3. DIGITAL DATA PROCESSING FOR TYPICAL CHANNELS

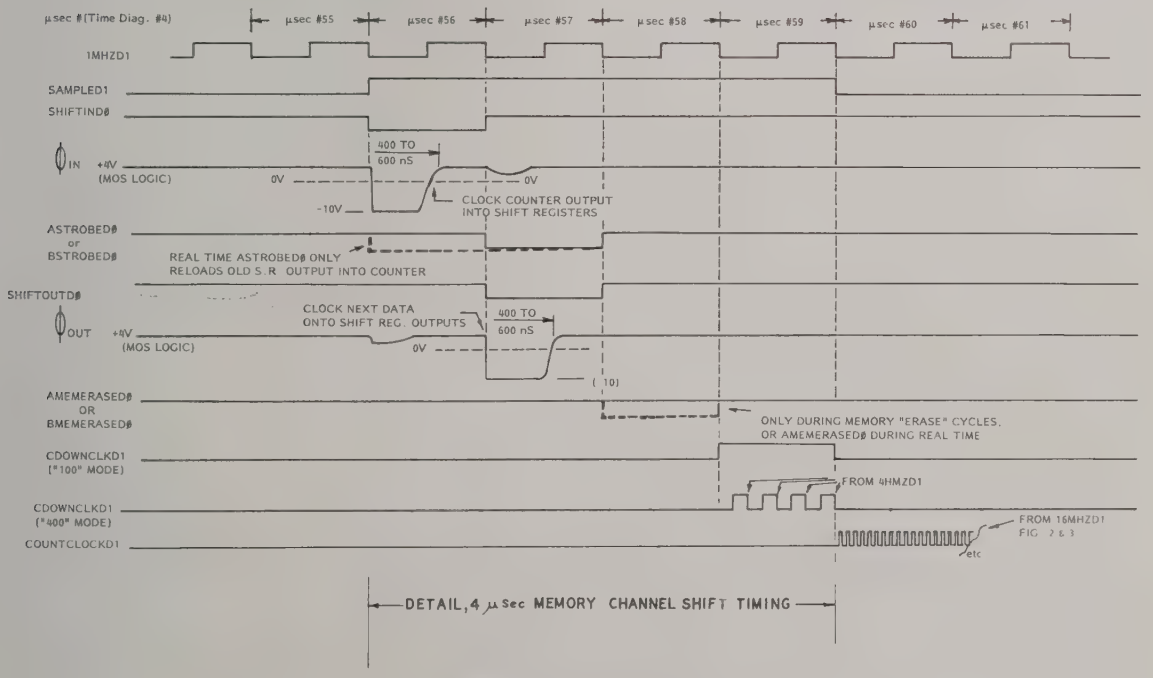


TIMING DIAGRAM #4

Figure XII-4. DETAIL, ONE 64 μSEC CHANNEL TIME

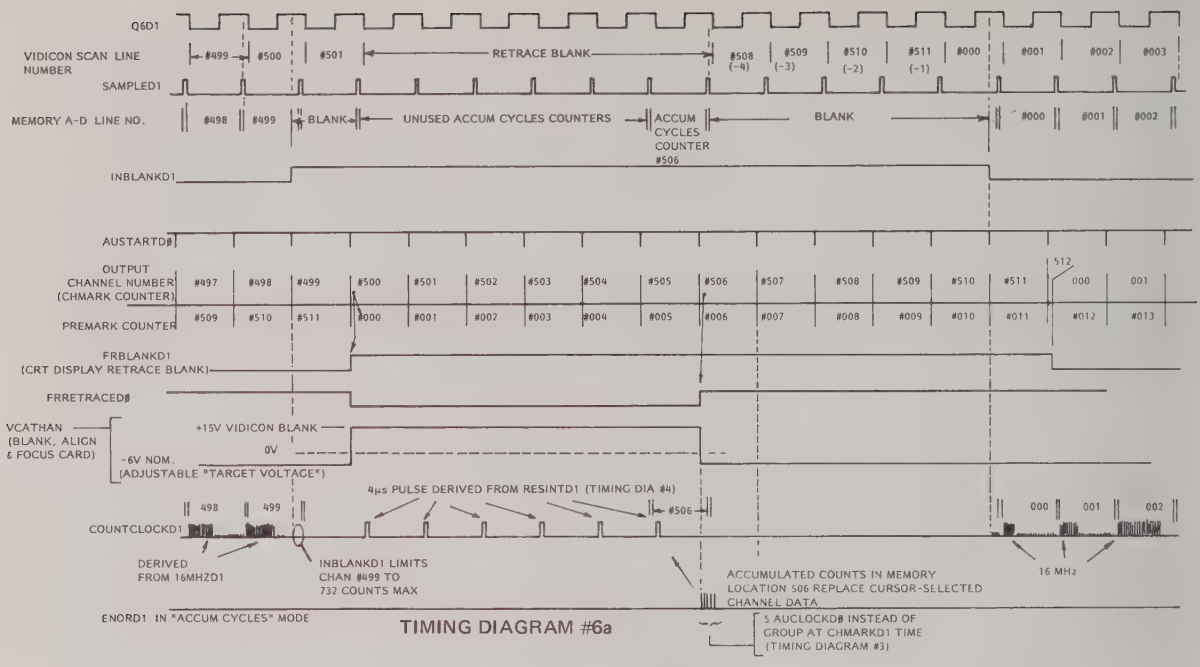


TIMING DIAGRAM #5a



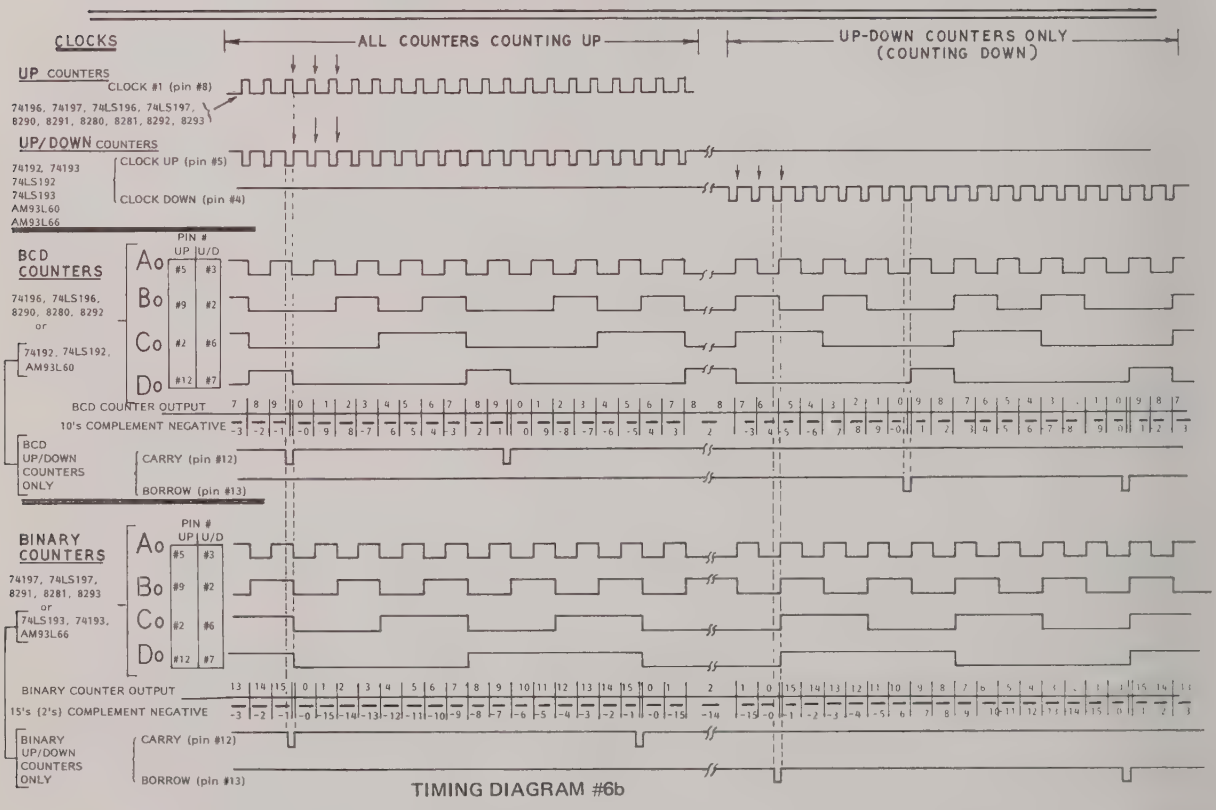
TIMING DIAGRAM #5b

Figure XII-5. DETAILS, ARITHMETIC CYCLE AND MEMORY TIMING



TIMING DIAGRAM #6a

DETAIL, FRAME BLANK INTERVAL



TIMING DIAGRAM #6b

Figure XII-6. DETAILS, FRAME BLANK INTERVAL AND COUNTER I.C. TIMING

12.2 SCHEMATICS

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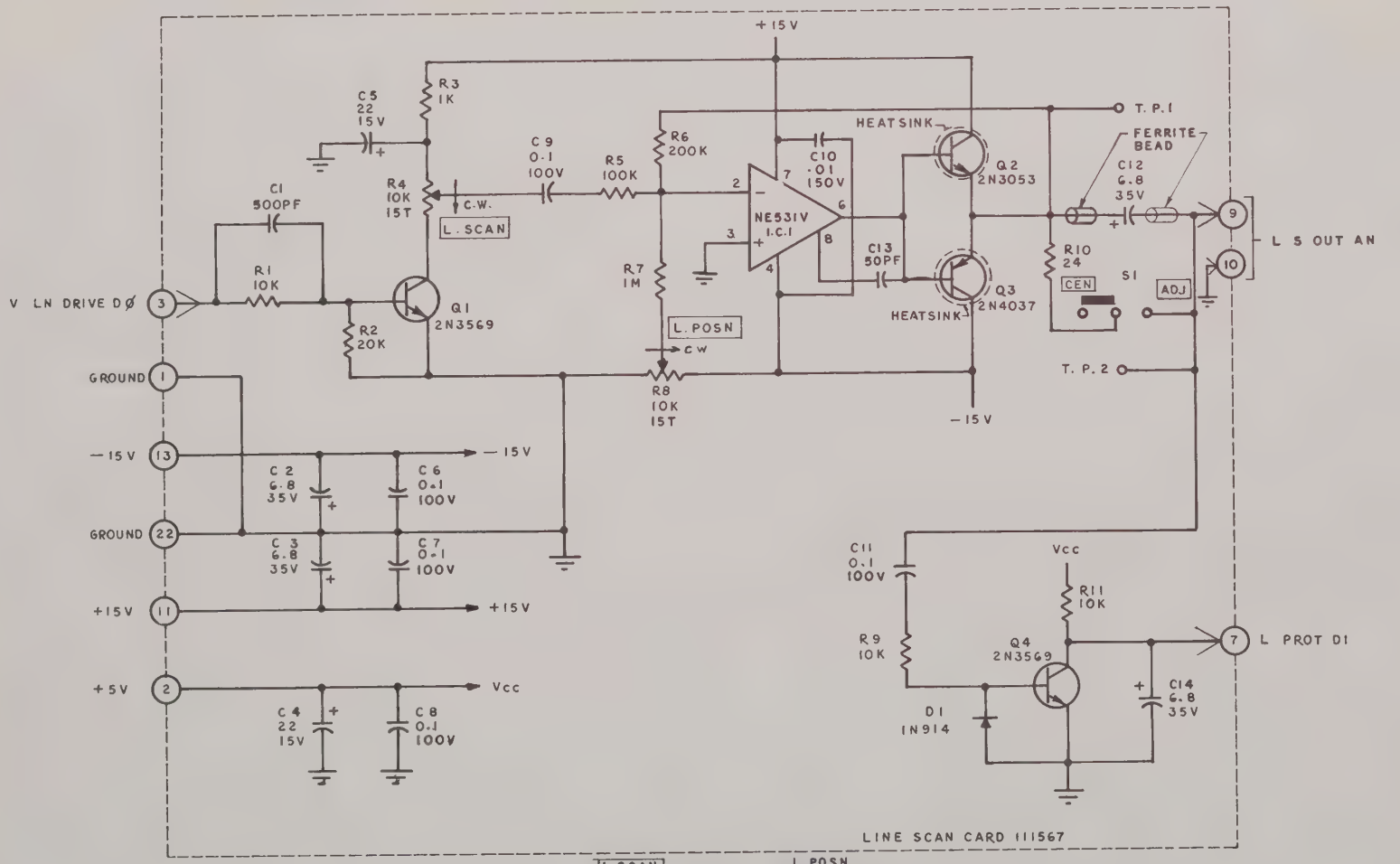
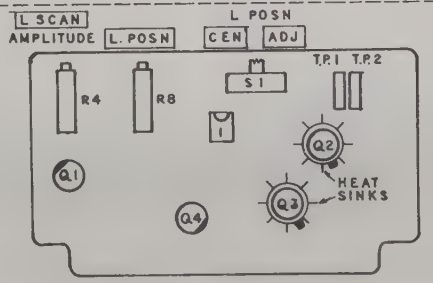
LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	JUNE 13-72			
B	ADDED FERRITE BEAD. DCN 3213	4-11-75	RNN		





2. RESISTORS ARE IN OHMS, 1/4W, 5%.
1. CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

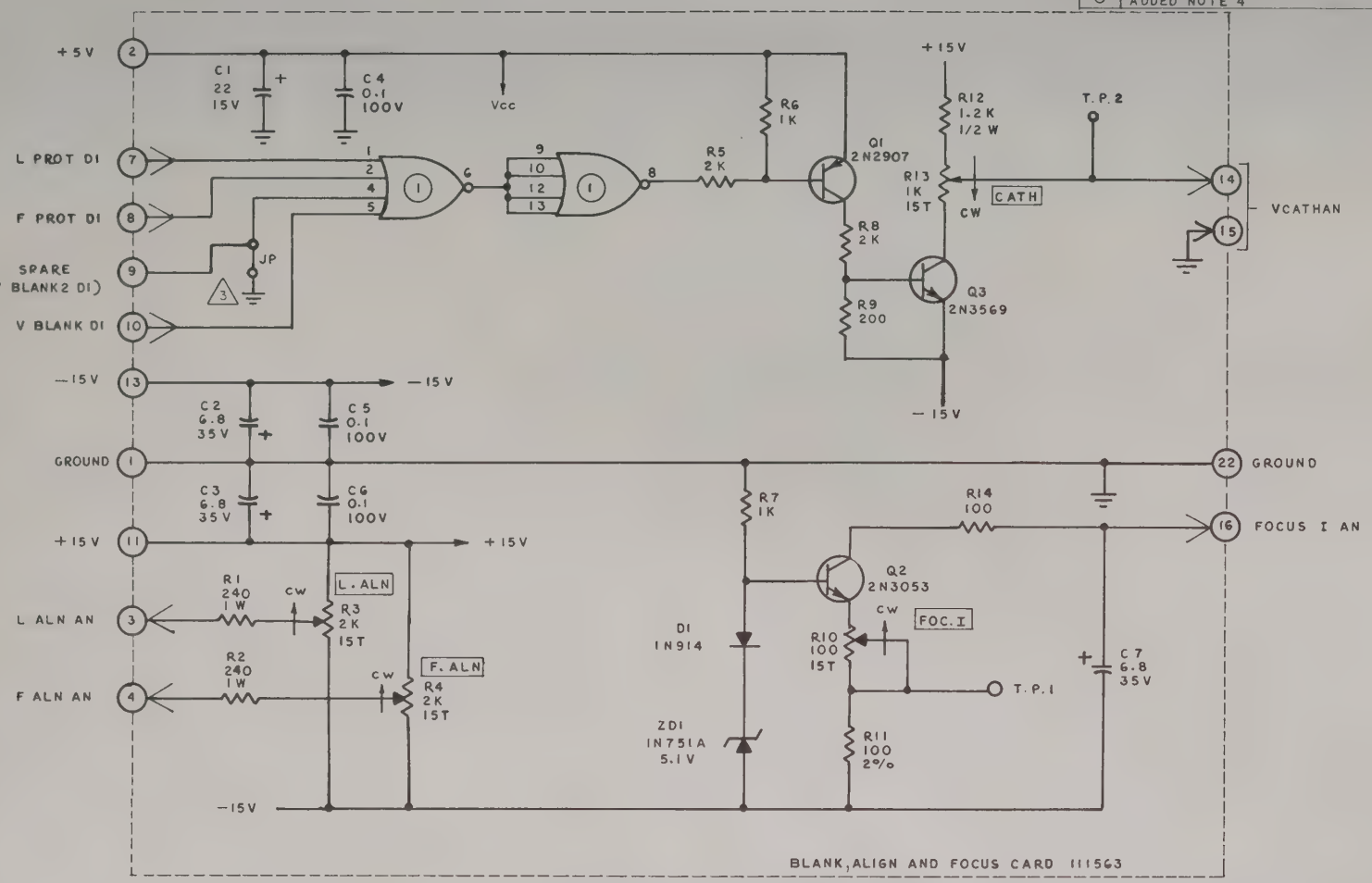
MATERIAL:
FINISH
DRAWN
CHECKED
APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±

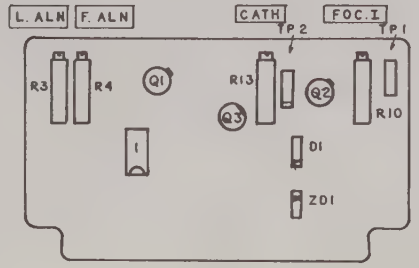
PRINCETON APPLIED RESEARCH

TITLE
LINE SCAN CARD SCHEMATIC

SCALE
DWG NO. 111537 B

LETTER	REVISION	DATE	DRAWN	CHKD	APR
D	CHANGED NOTE 4 TO NOTE 3 DCN 3213	4-1175	RVW		
B	R5 WAS 20K; R6 WAS 10K; R8 WAS 10K; R9 WAS 10K	MAR 28-73			
C	REMOVED NOTE 3; ADDED NOTE 4	JAN 4-74			





I.D.	PART NO.	Vcc	GND	TYPE
1	N8815A	14	7	DUAL 4-INPUT NOR

LIST OF MATERIALS

3. JUMPER REMOVED WHEN USING DUAL SPECTRUM INPUT CARD

2. RESISTORS ARE IN OHMS, 1/4W, ± 5%.

1. CAPACITORS ARE IN MICROFARADS.

NOTES EXCEPT AS NOTED

XII-11

MATERIAL:

FINISH

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

PRINCETON APPLIED RESEARCH

TITLE

BLANKING, ALIGNMENT AND FOCUS CARD SCHEMATIC

SCALE

DATE 1-5-72

DWG NO. 111535

D

XII-12

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	MAY 16-72			
B	SEE REVISION FILE	JUNE 14-72			
C	ADDED C12 AND R16	SEPT 19-72			
D	R10 & R13 WERE 1/4W; R12 & R13 WERE 3K; U1 & U2 WERE NS558V; CORRECTED ... FROM C3 ON SCH ASSY SKE-CH; ADDED WAVE FORM. 2/23/15	4-14-15	RNW		

111564

VFR RETRACE DI (3)

R1 1K

R5 20K

−15V

F. SCAN

Q1 2N2222

R7 10K CW

R9 1% 10K 1/8W

+15V

C7 1 100V POLYCARB.

R12 3.01K 1% 1/8W

R15 3.01K 1%, 1/8W

C12 .001

R2 30K 1% 1/8 W

R6 10K 1%, 1/8W

C8 .01

C9 .01

R8 10K 1% 1/8W

R10 681 1% 1/8 W

R13 681 1%, 1/8 W

TEST POINT

R16 200

GROUND (1)

−15V (13)

GROUND (22)

+15V (11)

+5V (2)

C1 6.8 35V

C2 6.8 35V

C4 0.1 100V

C5 0.1 100V

C3 22 15V

C6 0.1 100V

Vcc

D1 IN936 9.0V

R4 10K CW

F POSN

R3 1K

−15V

+4.1V

0V

-4.1V

-9V

C10 0.47 50V

Vcc

R14 10K

R11 3.9K

Q2 2N3569

C11 200 6V

D2 IN914

(6)

(7) — FRS OUT AN

(8) F PROT DI

I.D.	PART NO	GND	+15V	-15V	TYPE
1, 2	NS558V or SN72558P	—	8	4	DUAL OPAMP

F. POSN

TEST POINT

F. SCAN AMPLITUDE

C7

C12

R16

Q1 Q2

D2

R8 R14 R11

1 22

2. RESISTORS ARE IN OHMS, 1/4 W, 5%.

1. CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± FRAC ±

2 PL DEC ± ANGLES ±

PRINCETON APPLIED RESEARCH

TITLE

FRAME SCAN CARD SCHEMATIC

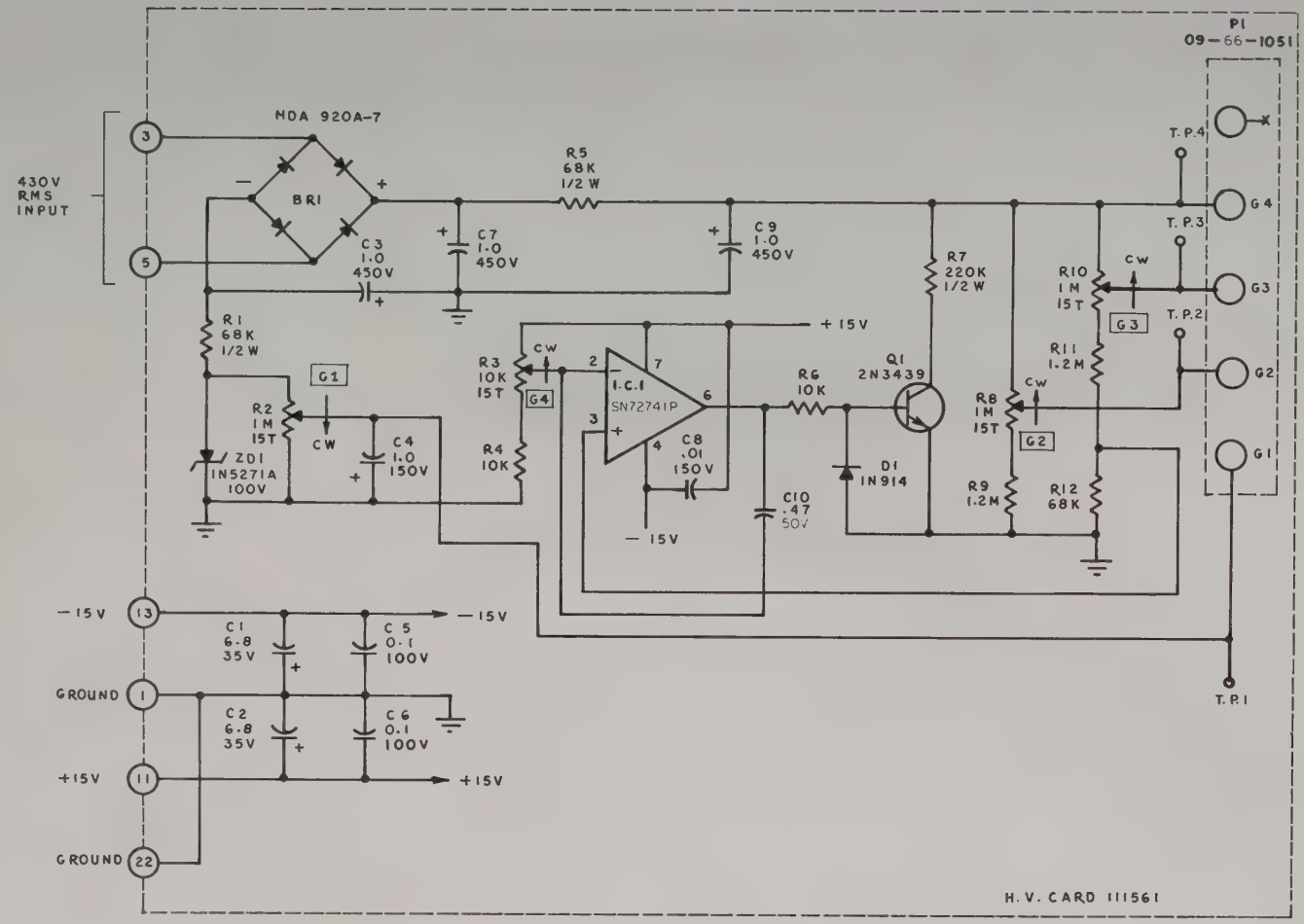
SCALE

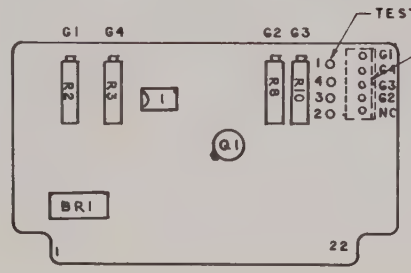
DATE 5-16-72

DWG NO. 111536

D

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	JUNE 13-72			
B	I.C. 1 WAS NS741V, C10 WAS 100V; P1 WAS 09-55-1051. DCN 3213	4-9-75	RNW		





NOTES: EXCEPT AS NOTED

1. CAPACITORS ARE IN MICROFARADS.
2. RESISTORS ARE IN OHMS, 1/4W, 5%.

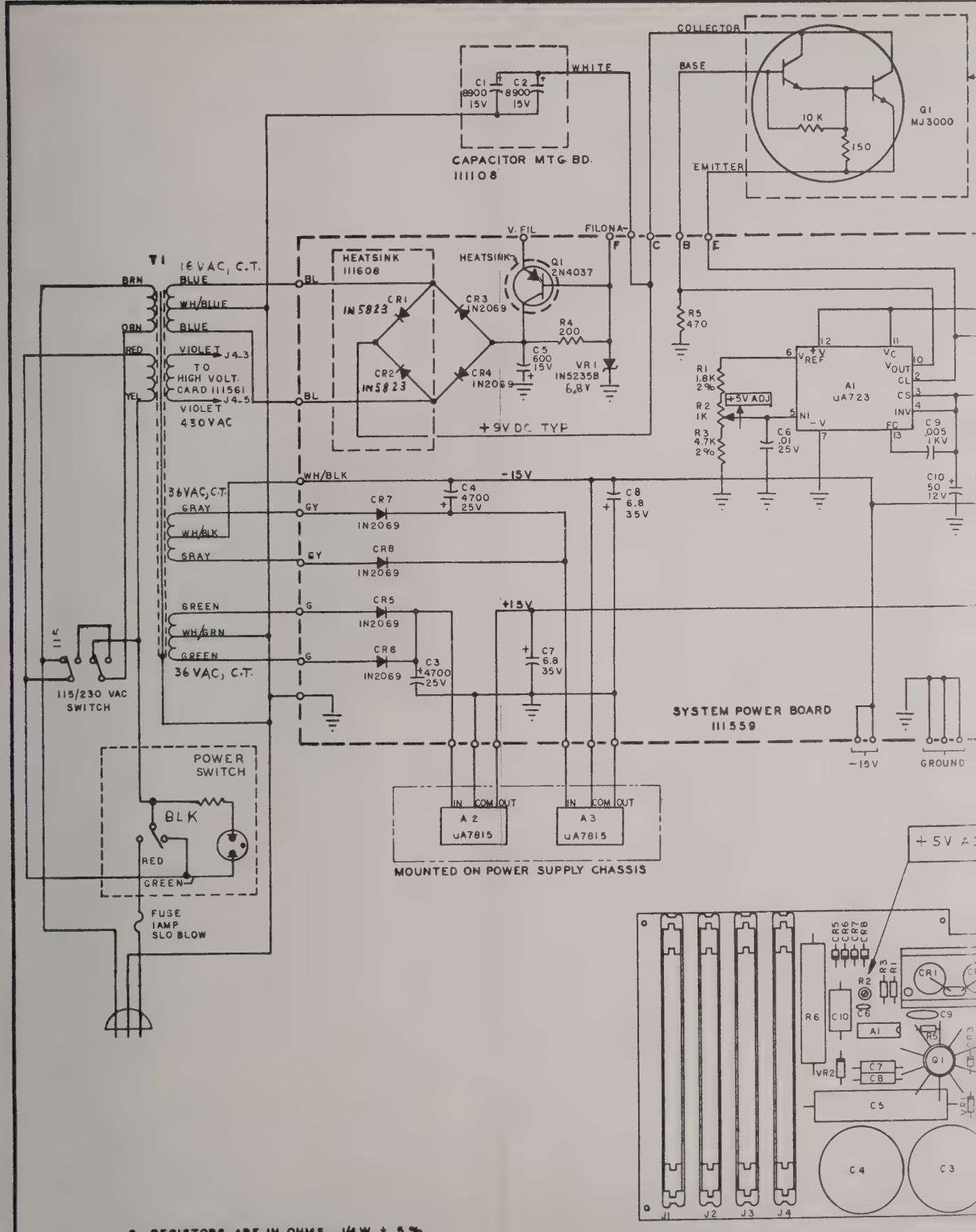
REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:
FINISH:
DRAWN
CHECKED
APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±

PRINCETON APPLIED RESEARCH

TITLE
HIGH VOLTAGE CARD SCHEMATIC

SCALE
DWG NO. 111574 B



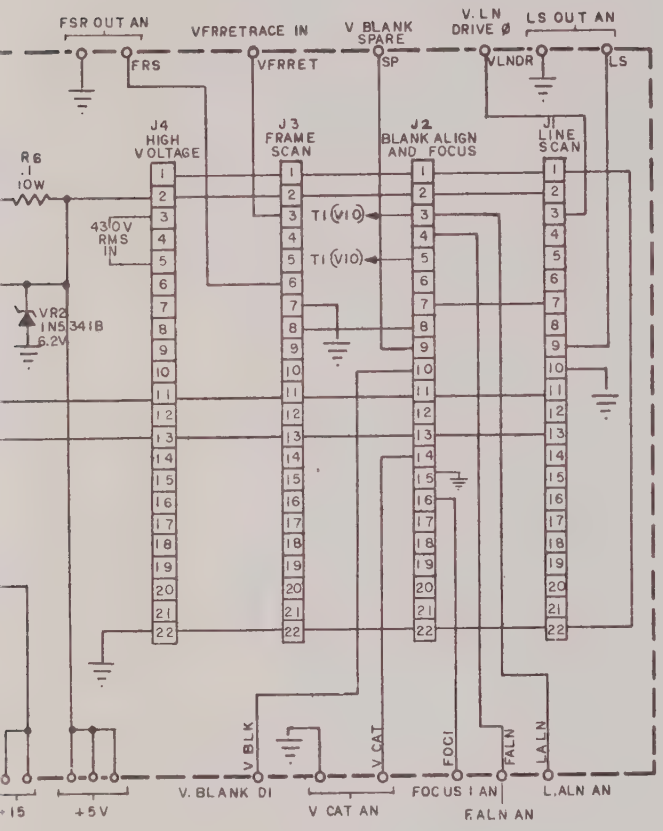
2 RESISTORS ARE IN OHMS, 1/4W, ± 5%.

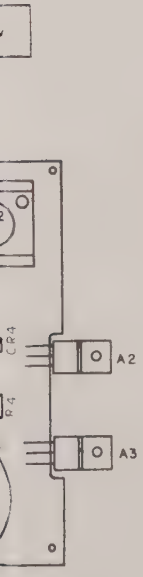
XII-14 1 CAPACITORS ARE IN MICROFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED

LETTER	REVISION	DATE			
B	REVISED & REDRAWN	9-21-73			
C	SEE REV FILE	JAN 7-74			
D	CR1 & 2 WERE MRD 5300 DC.V 3213	1-10-75	RNW		

HEATSINK AND TRANSISTOR ON REAR PANEL





REF DESIGNATIONS	
LAST NO. USED	NUMBERS NOT USED
A3	
C10	C1, C2
CR8	
J4	
Q1	
R6	
VR2	

REQD	PART NO.	DESCRIPTION	ITEM
LIST OF MATERIALS			

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

Princeton Applied Research Corporation
Princeton New Jersey

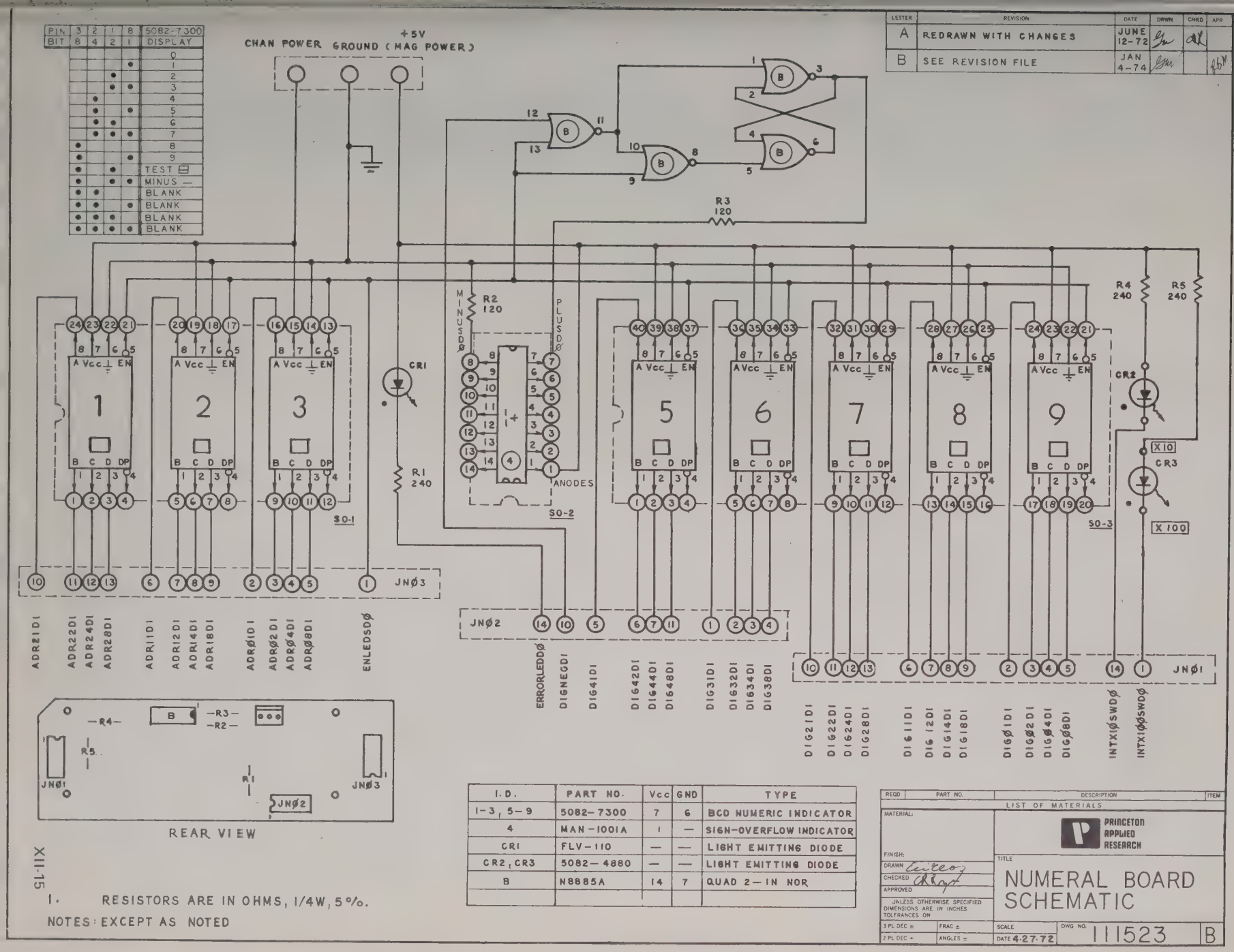
TITLE
SCHEMATIC
SYSTEM POWER BOARD

SCALE none

DATE 9-21-73

DWG NO. 111533

D



LETTER	REVISION	DATE	DRWN	CHKD	APP
A	REDRAWN WITH CHANGES	JUNE 12-72			
B	SEE REVISION FILE	JAN 4-74			

REAR VIEW

I.D.	PART NO.	Vcc	GND	TYPE
1-3, 5-9	5082-7300	7	6	BCD NUMERIC INDICATOR
4	MAN-1001A	1	—	SIGN-OVERFLOW INDICATOR
CR1	FLV-110	—	—	LIGHT EMITTING DIODE
CR2, CR3	5082-4880	—	—	LIGHT EMITTING DIODE
B	N8885A	14	7	QUAD 2-IN NOR

XII-15

1. RESISTORS ARE IN OHMS, 1/4W, 5%.

NOTES: EXCEPT AS NOTED

REQD | PART NO. | DESCRIPTION | ITEM

LIST OF MATERIALS

MATERIAL:

FINISH:

DRAWN Enrico

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ± | ANGLES ±

2 PL DEC ±

PRINCETON APPLIED RESEARCH

TITLE

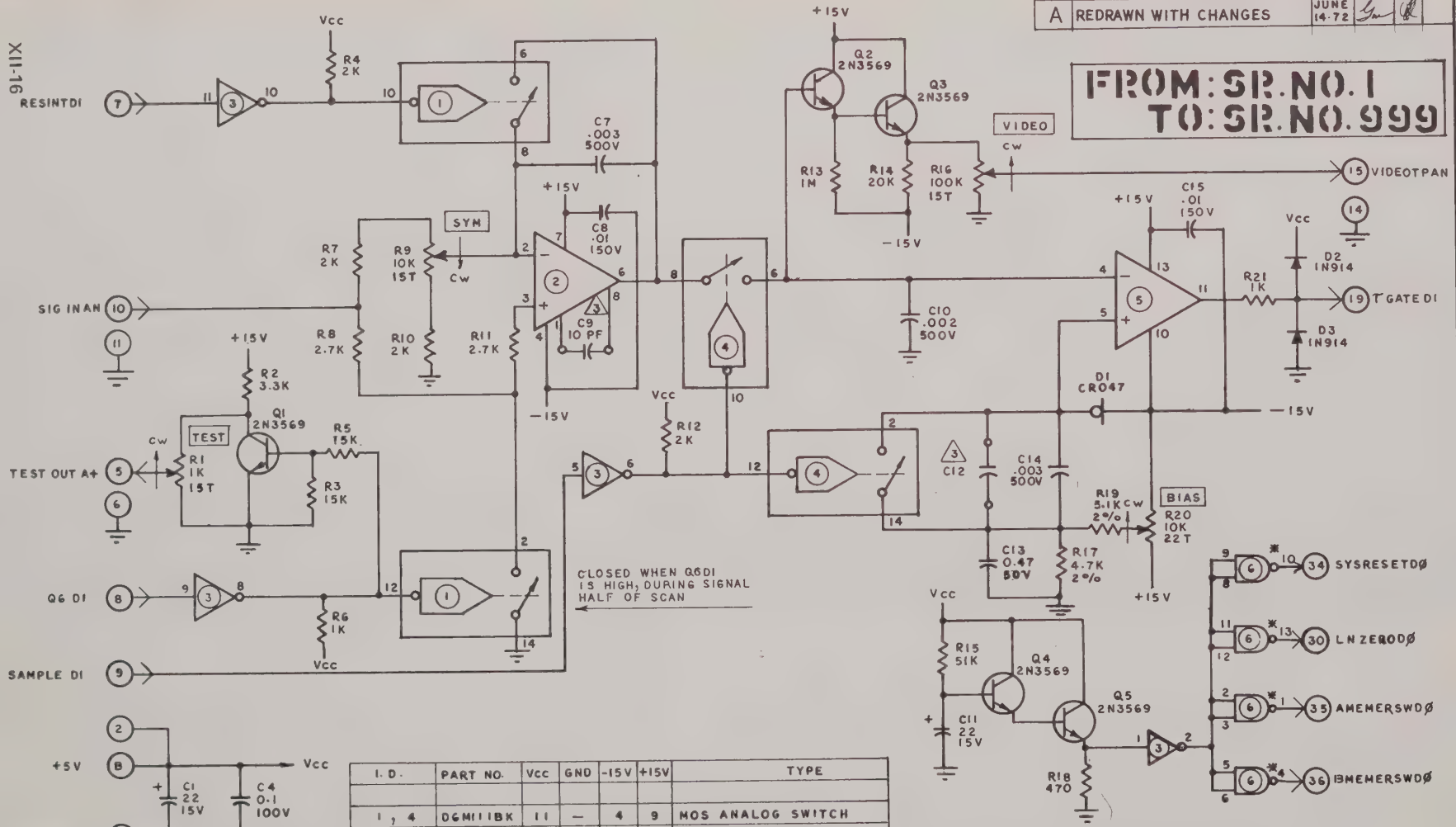
NUMERAL BOARD SCHEMATIC

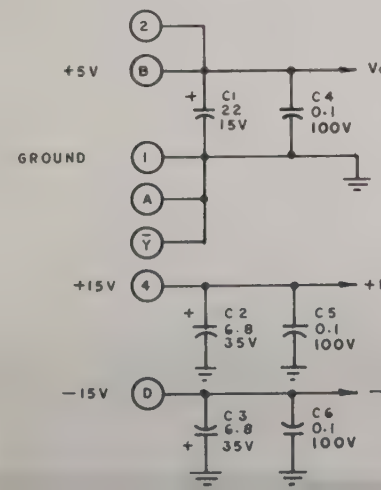
SCALE | DWG NO. 111523 | B

DATE 4-27-72

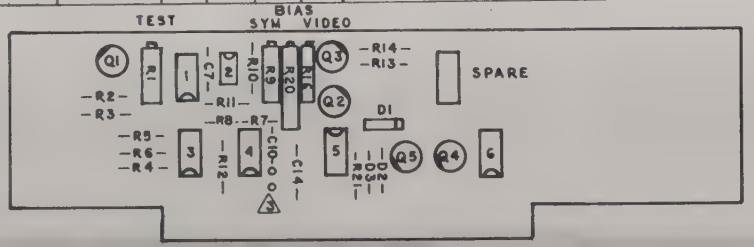
LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	JUNE 14-72			

FROM: SR. NO. 1
TO: SR. NO. 999





I. D.	PART NO.	Vcc	GND	-15V	+15V	TYPE
1, 4	DGM111BK	11	—	4	9	MOS ANALOG SWITCH
2	N5556V	—	—	4	7	OPAMP
3	N8890A	14	7	—	—	HEX INVERTER
5	μA715C	—	—	10	13	OPAMP
6	N8881A	14	7	—	—	QUAD 2-INPUT NAND, OPEN COLL



△3 SELECTED DURING TEST.
2. RESISTORS ARE IN OHMS 1/4 W 5%.
1. CAPACITORS ARE IN MICROFARADS.
NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:
FINISH:
DRAWN
CHECKED
APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±
2 PL DEC ± ANGLES ±

PRINCETON APPLIED RESEARCH

TITLE
INPUT CARD SCHEMATIC

SCALE
DWG NO. 111525 A
DATE 1-20-72

LETTER	REVISION	DATE	DRAWN	CHKD	APPD
A	SEE REV FILE				
B	I.C. 8 WAS N8890A, I.C. 2 WAS N8890A, C15 THRU 18 WERE .33V 20% 50V	8/7/75	DMS		

RESINTD1 (7) → N8890A (2a) → R1 2K → Vcc

DGM111BK (1a): C1 .003±5% 500V MICA; R2 10K±2%

TP1 — SIGINAN (10) — SIG/POW #2 PREAMPOUTAN — TEST — TEST OUT A+ (5, 6)

R3 5.1K ±2%

TP2 — R4 10K±2% — R5 5.1K±2%

+15V — (3) N5556V — R9 10K — SYMMETRY — R11 2K 15T CW — R12 1.5K±2% — C2 .01,150V — −15V

CLOSED = Q6D1 LOW

(4) N5556V — C3 .01,150V

TP3 — TP4 — (5b) — C4 .002 ±5% 500V MICA

R13 15K±2%

+5V — 27Ω — TEST

R10 3.3K — TEST — R15 1K 15T CW — R16 1K — R17 2K — Vcc

(1b) — (2d)

CHMARKD1 (27) — (2b) — R18 10K — Q3 — Q4 — R19 10K — R20 10K — R21 10K — (2f)

TP7 — HIGH = SIGNAL = INTEGRATE UP

Q6D1 (8)

SAMPLED1 (9)

+5V (2, B) — C9 22,15V — C10 0.1,100V — Vcc

+15V (4) — C11 6.8,35V — C12 0.1,100V — +15V

−15V (D) — C13 6.8,35 — C14 0.1 100V — −15V

GND (I, A, Y)

Vcc — R22 2K — (2a) — (5a)

TP6

−15V — R23 1K — VR1 IN751A 5.1V — C15 .1, 50V

RAMP — R24 6.8K±2% — CW — R25 5K 15T

BIAS — R26 10K 22T — CW — C17 .01 150V

VR2 IN751A 5.1V — C16 .1, 100V

VR3 IN751A 5.1V — C18 .1 100V

R27 2K — +15V

+15V — C6 .003±5%, 500V MICA — C7 100PF, 100V — (7) NE531V — C8 .01,150V — −15V

Vcc — R28 51K — Q5 — C19 22 15V — Q6 — R29 470

Q1 — Q2 — R6 1M — R7 20K — R8 100K 15T CW — VIDEO — VIDEOTPAN (15, 14) — VIDEO BNC

+15V — (6) UA715C — R14 1K — CR1 IN914 — TP5 — (19) Y GATE D1 — CR2 IN914 — C5 .01,150V — −15V

Vcc

N8881A

(8a) → (34) SYSRESETDØ

(8d) → (30) LNZERODØ

(8c) → (35) AMEMERSWSWDØ

(8b) → (36) BMEMERSWDØ

(2c)

1205A INPUT CARD — SPARE — 111612 LAYER 1

Q6D1: HI=SIG — TP7 — GND — TEST — SYM — INPUT — INVERTER — INTEGRATE — SAMPLE-HOLD — T GATE — RAMP — VIDEO — BIAS

REF DESIGNATION	
HIGHEST NO. USED	NO. NOT USED
R29	
C19	
CR2	
VR3	
Q6	
IC8	
TP7	

2	SN7420N	14	7	QUAD 2-INPUT NAND
7	NE531V	—	—	OP AMP
6	UA715C	—	—	OP AMP
3,4	N5556V	—	—	OP AMP
1,5	DGM111BK	11	—	MOS ANALOG SWITCH
2	SN7404N	14	7	HEX INVERTER

IDENT	PART NO.	Vcc	GND	TYPE

LIST OF MATERIALS

5. * DENOTES OPEN COLLECTOR.
4. DGM111BK PIN 9 IS +15V AND PIN 4 IS −15V.
3. TRANSISTORS ARE 2N3569.
2. RESISTORS ARE IN OHMS ±5%, 1/4W.
1. CAPACITORS ARE IN MICROFARADS ±10%.

NOTES—UNLESS OTHERWISE SPECIFIED

MATERIAL:
FINISH:
DRAWN
CHECKED
APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ±
2 PL DEC ±
FRAC ±
ANGLES ±

INPUT CARD—SCHEMATIC (1000 SERIES AND UP)

XII-17

SCALE NONE
DATE 9-26-72
DWG NO. 111610
5

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	JUNE 13-72			
B	I.C. 6,14,17,20,24 WERE N7474A	JAN 3-74			

I.D.	PART NO	Vcc	GND	TYPE
1	N8870A	14	7	TRIPLE 3-INPUT NAND
2	N7474A	14	7	DUAL 'D' TYPE FLIP FLOP
3,7	N8816A	14	7	DUAL 4-INPUT NAND
4	N8281A/DC	14	7	4 BIT BINARY COUNTER
5,11	N74107A	14	7	DUAL J-K FLIP FLOP
8,12,15,18,19,22	N8880A	14	7	QUAD 2-INPUT NAND
9,13,21,23,25	N8885A	14	7	QUAD 2-INPUT NOR
10	N7495A	14	7	4 BIT SHIFT REGISTER
16	N8875A	14	7	TRIPLE 3-INPUT NOR
6,14,17,20,24	SN74LS74N	14	7	DUAL 'D' TYPE FLIP FLOP

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ±	FRAC ±	SCALE	DWG NO. 111524
2 PL DEC ±	ANGLES ±	DATE 2-24-72	6

Princeton Applied Research Corporation
Princeton, New Jersey

TITLE

TIMING CARD SCHEMATIC

NOTES: EXCEPT AS NOTED
1. CAPACITORS ARE IN MICROFARADS
2. RESISTORS ARE IN OHMS, 1/4 W, 5%.

5-15-72

LETTER	REVISION	DATE	DRWN	CHKD	APP
C	C1, C2 WERE .1 MFD, 100V. IC 28 WAS N8880A, IC'S 29,30,32,33,35 WERE N8881A, IC 31 WAS SN74107A DCN 3213	4-1-75	RWW		

SHIFT IN DØ (6)
SHIFT OUT DØ (7)
C1 1.8nF
C2 1.8nF
R2 10
R3 10
C3 .01 100V
-12V
Vcc
ZD1 IN5225B
-15V (D)
3.0V
R1 2K
C4 0.1 100V
C5 22 15V
-12V
A/B COUNTENADI (8)
COUNT CLOCK DI (9)
MEMORY COUNTING REGISTER
A/B STROBE DØ (10)
A/B MEM ERASE DØ (11)
TØDI (12)
(N)
(2)
+5V (B)
GROUND (1)
(A)
(Y)
OUTPUT MPX
C6 22 15V
C7 0.1 100V
C8 0.1 100V
C9 0.1 100V
C10 0.1 100V
C11 0.1 100V
Vcc
SHIFTINDØ
+5
0
300µs
Ø IN
+4
-10
Ø OUT
512 WORD SHIFT REG (IC'S 1–21)
SIGN BIT
A/B COUNTENADI
100'S CARRY CLOCK
SPARE
R4 510
R5 510
R6 510
R7 510
A/BØ1 DØ
A/BØ2 DØ
A/BØ4 DØ
A/BØ8 DØ
A/BØ4ØØ
A/B MEMERASEDI
13 TIDI (P)
U 8MHZDI
17 COUNTCLKDI
T2DI (R) 14
15 T3DI (S)
A/B FULL DØ 29
16 (T) T4DI

I.C.	PART NO.	Vcc	GND	-12V	TYPE
1 – 21	MM5016N	4,6	—	8	512 BIT SHIFT REGISTER
22 23	N8280A/DC	14	7	—	4 BIT BCD COUNTER
24–26	N74192B	16	8	—	4 BIT UP/DOWN BCD COUNTER
27	MH0025CN	6	—	3	CLOCK DRIVER TTL–MOS
28	SN74H00N	14	7	—	QUAD 2–IN NAND
29, 30, 32, 33, 35	SN7401N	14	7	—	QUAD 2–IN NAND (OPEN COLL = *)
31	SN74107N	14	7	—	DUAL J–K FLIP FLOP
34, 36	N8816A	14	7	—	DUAL 4–IN NAND
37	N8880A	14	7	—	QUAD 2–IN NAND

3. A/B MEANS A OR B DEPENDING UPON CARD LOCATION.
2. RESISTORS ARE IN OHMS, 1/4W, 5%.
1. CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM

LIST OF MATERIALS

MATERIAL:
FINISH:
DRAWN Rukeyser
CHECKED
APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±
2 PL DEC ± ANGLES ±

Princeton Applied Research Corporation
Princeton, New Jersey

TITLE
MEMORY CARD SCHEMATIC
XII-19

SCALE
DATE 1-18-72
DWG NO. 111526
C

LETTER	REVISION	DATE	DRWN	CHKD	APP
A	REDRAWN WITH CHANGES	JUNE 13-72			
B	I.C. 12 & 13 WERE SN7483N	JAN 8-74			
C	I.C. 2 & 14 WERE N8830A; I.C. 10 WAS N8815A. DCN 3213				

AØ4BØ

AØ1DØ
AØ2DØ
AØ4DØ
AØ8DØ

BØ4BØ

BØ1DØ
BØ2DØ
BØ4DØ
BØ8DØ

ADDER

BORROW ADD TEN ADDER

ARITHNEGØI

ENDDIGDØ

74H87

CONTROL		OUT
B	C	
0	0	A+B
0	1	A-B
1	0	B
1	1	0

CARRY FLIP FLOP

ZERØDI

CØ1DI
CØ2DI
CØ4DI
CØ8DI
CØ4BI

T1DI
T2DI
T3DI
T4DI
TØ5BI
TØDI

AUBUSYDI

MIDDI6DI

AUCLOCKDØ

SPARES

BMHZDI

AUSTARTDØ

INIT. RDI

CYCLEIDI

RUN

SUBTRACT

ANEGDI
BNEGDI
REALSWDØ
ASWDØ
BSWDØ

ASIGN ≠ BSIGN

ATRANSFER

BTRANSFER

SIGN

ARITHNEGDI

+5V
GROUND

C1 22 15V
C2 0.1 100V
C3 0.1 100V
C4 0.1 100V
C5 0.1 100V
C6 0.1 100V
C7 0.1 100V

ZERØDI
CYCLEIDI
MIDDIGDI
Vcc

LEADING ZERO COUNTER

DACE4DI
DACE2DI
DACE1DI

LOGDI

LOGSWDØ

SCALEIØ-2DI
SCALEIØ-1DI

I. D.	PART NO.	Vcc	GND	TYPE
1	N8870A	14	7	TRIPLE 3-INPUT NAND
2,14	[illegible]	14	7	HEX INVERTER
3	N74107A	14	7	DUAL J-K FLIP FLOP
4	N7474A	14	7	DUAL 'D' TYPE FLIP FLOP
5	N8885A	14	7	QUAD 2-INPUT NOR
6	N8281A/DC	14	7	4 BIT BINARY COUNTER
7	N8816A	14	7	DUAL 4-INPUT NAND
8,10	N8880A	14	7	QUAD 2-INPUT NAND
9	N8280A/DC	14	7	4 BIT BCD COUNTER
11	N8271B	16	8	4 BIT SHIFT REGISTER
12,13	SN74LS83N	5	12	4 BIT FULL ADDER
15	N8241A	14	7	QUAD 2-IN EXCLUSIVE OR
16	SN74153N	14	7	DUAL 4-INPUT NOR
17,18	SN74H87N	14	7	4 BIT LOGIC ELEMENT

1 CAPACITORS ARE IN MICROFARADS.
NOTES: EXCEPT AS NOTED.

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:
FINISH:
DRAWN
CHECKED
APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±
2 PL DEC ± ANGLES ±

Princeton Applied Research Corporation
Princeton New Jersey

TITLE
ARITHMETIC CARD SCHEMATIC

SCALE
DATE 1-24-72
DWG NO. 111528

LETTER	REVISION	DATE	DRWN	CHKD	APP'D
A	REDRAWN WITH CHANGES	JUNE 14-72			
B	CHANGED PER ECO 1003	JAN 8-74			
C	RSERB WERE 220K, 2% U4 WAS N7405A, DCN 3213	4-4-75	RMA		

+15V
-15V
C1 6.8 35V
C2 6.8 35V
C4 0.1 100V
C5 0.1 100V

FRONT PANEL
CW
VERT EXPAND
CAL
LOG
10K
1.1K
10K 2%
1.1K 2%
J6 25
J6 41 MOTHER BOARD
DACOUTA+
DAC A+

C0 1D1
C0 2D1
C0 4D1
C0 8D1
C0 4BI
AUCLOCKD0
T0D1
T1D1
T2D1
T3D1
T4D1
T5BI
DACE4D1
DACE2D1
DACE1D1
DACE3BI
ARITHNEGD1
LOGD1

Vcc
R1 2K
R2 2K
R3 2K
R4 2K
INH EN1 EN2
I7 I6 I5 I4 I3 I2 I1 I0
S2 S1 S0
01 02 0Ø

DA DB DC DD S
AO BO CO DO R
.01 ANALOG OUT
.02
.04
.08
0-10V
0.1
0.2
0.4
0.8
MSD1
MSD2 REFIN
MSD4 REFOUT
MSD8
+15V
-15V

R5 221K 1% 1/8W
R6 150K
R7 150K
R8 221K 1% 1/2W
C11 .01 150V
R9 12K
LOG GAIN
R10 10K
R11 3K
LINEAR GAIN
R12 10K
LINEAR POSITION
R13 10K
R14 33K
R15 2K
R16 4.3K
C12 .01 150V
R21 1K
R22 1K
ZD1 IN5225 3V
ZD2 IN5225 3V
SAMPLEYAN
CRTY

R17 39K
R18 10K
R19 15K
R20 10K
LOG EXPONENT
R23 11K
C13 .47 50V
R24 470K
R25 470K
C14 .01 150V

A1 A2 A3 A4 A5 A6
IO -REF +REF COMP V+ V-
C10 50PF

I.C. 1 TRUTH TABLE						
INHIBIT	S0	S1	S2	O0	O1	O2
0	0	0	0	$\overline{I0}$	$\overline{I1}$	$\overline{I2}$
0	1	0	0	$\overline{I1}$	$\overline{I2}$	$\overline{I3}$
0	0	1	0	$\overline{I2}$	$\overline{I3}$	$\overline{I4}$
0	1	1	0	$\overline{I3}$	$\overline{I4}$	$\overline{I5}$
0	0	0	1	$\overline{I4}$	$\overline{I5}$	$\overline{I6}$
0	1	0	1	$\overline{I5}$	$\overline{I6}$	$\overline{I7}$
0	0	1	1	$\overline{I6}$	$\overline{I7}$	1
0	1	1	1	$\overline{I7}$	1	1
1	X	X	X	1	1	1

I D.	PART NO.	Vcc	GND	-15V	+15V	TYPE
1	N8243N	24	12	—	—	8 BIT POSITION SCALER
2, 6, 9	N8292A	14	7	—		4 BIT BCD COUNTER
3	CY2635	18	8,31	33	32	BCD D/A CONVERTER
4	[illegible]	14	7	—	—	QUAD 2-INPUT AND
5	MC1406L	11	2	3	—	D/A CONVERTER
7	N8880A	14	7	—	—	QUAD 2-INPUT NAND
8	N5558V	—	—	4	8	DUAL OPERATIONAL AMP.
10	DGM111BK	11	—	4	9	MOS ANALOG SWITCH
11	N5556	—	—	4	7	OPERATIONAL AMP.

+5V
GROUND
C3 22 15V
C6 0.1 100V
C7 0.1 100V
C8 0.1 100V
C9 0.1 100V
Vcc

LINEAR GAIN
LOG EXPONENT
LINEAR POSITION
LOG GAIN
EX LIN POS LOG G
R18 R12 R13 R10
SPARE

2. RESISTORS ARE IN OHMS 1/4W 5%.
1. CAPACITORS ARE IN MICROFARADS.
NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:
FINISH:
DRAWN
CHECKED
APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±
2 PL DEC ± ANGLES ±

TITLE
OUTPUT CARD SCHEMATIC
XII-21

SCALE
DATE 2-27-72
DWG NO. 111521
5-13-73

LETTER	REVISION	DATE	DRWN	CHKD	APP
A	REDRAWN WITH CHANGES R11 DELETED	JUNE 13-72			
B	R32 WAS 5.1K, R33 WAS 2.2K, R34 WAS 3.9K	12-6-74	DUN		
C	R19 & R38 WERE 250Ω - DCN 3213	4-2-75	RNW		

SAMPLEYAN

PLOTY

+15V

+15V

-15V

-15V

R10 10K

R19 249 1%

C10 .01 150V

C11 .47

C12 .01 150V

Q1 2N3569

R16 2K

MARKDØ

Vcc

R12 10K

P/PSWDØ

+15V

-15V

C1 6.8 35V

C4 0.1 100V

C2 6.8 35V

C5 0.1 100V

+15V

-15V

FRBLANKDI

R1 10K

Vcc

C6 0033 200V MYLAR

CHMARKDI

AUSTARTØ

-TIMING-

R5 100K 15T

Z LEVEL

R7 22K

R13 3.9K

R8 5.1K

R2 50K 15T

Z BLANK

R3 22K

Z MARK

R4 100K 15T

R6 100K 15T

Z COMP

R9 39K

MARKDØ

INTENA-

C9 .01 150V

R14 1K

R15 1K

S1

-Z HIGH +

R17 3.3K

R18 3.3K

R20 100K 15T

Z HIGH

CRT Z HIGH

CRT X

CRT Y

INTENA-

R21 20K

R24 2K

C14 0.1 200V MYLAR

R25 180K

R26 1.2M

R27 180K

R28 100K.1T CRT X RAMP TRIM

C13 6.8 35V

R34 510

R36 510

ZD1 IN5225

HOREXA-

RCRTXDØ

P/PSWDØ

SLOMODEDI

Vcc

R29 2K

R35 100

C15 1.0 100V POLYCARBONATE

PLOT RAMP TRIM

R30 10K 20T

Q2 2N3638A

R22 12K

R23 100K

R31 68K

R33 5.1M

C16 .01 150V

R37 1.21K 1%

R38 249 1%

PLOTX

+5V

GROUND

C3 22 15V

C7 0.1 100V

C8 0.1 100V

Vcc

EXPANDED Z COMP ENSATE

Z MARK

Z LEVEL

Z BLANK

CRT X RAMP WIDTH

Z HIGH GAIN

-Z HIGH+ POLARITY

X RAMP R29

PLOT RAMP

R30

PLOT X RATE

3. RESISTORS — R37, R38, R19 METAL FILM.

2. RESISTORS ARE IN OHMS, 1/4W, 5%.

1. CAPACITORS ARE IN MICRO-FARADS.

NOTES: EXCEPT AS NOTED.

I.D.	PART NO.	Vcc	GND	-15V	+15V	TYPE
1	SN74121N	14	7	—	—	ONE SHOT MULTIVIBRATOR
2	N8680A	14	7	—	—	QUAD 2-INPUT NAND
3,8	N5558V	—	—	4	8	DUAL OPEPATIONAL AMP.
4,5	DGM111BK	11	—	4	9	MOS ANALOG SWITCH
6,7	N5556V	—	—	4	7	OPERATIONAL AMPLIFIER

REQD | PART NO. | DESCRIPTION | ITEM

LIST OF MATERIALS

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

Princeton Applied Research Corporation

TITLE

DISPLAY DRIVE CARD SCHEMATIC

SCALE

DATE 2-27-72

DWG NO. 111531-B-SD

LETTR	REVISION	DATE	DRWN	CHKD	APR.
A	[illegible]	[illegible]			
B	N74193 (1-C.22) WAS N74192B	SEPT 20-72			
C	I.C. 1, 10, 14, 17, 24 WERE N7474A I.C. 22 WAS N74193. ADDED NOTE 3	JAN 9-74			

I.D.	PART NO.	Vcc	GND	TYPE
1,10,14,17,24	SN74LS74N	14	7	DUAL 'D' TYPE FLIP FLOP
2, 11, 19	N8880A	14	7	QUAD 2-INPUT NAND
3, 23	SN7425N	14	7	DUAL 4-INPUT NOR
4, 12	N74107A	14	7	DUAL J-K FLIP FLOP
5, 6	N8292A	14	7	4 BIT BCD COUNTER
7	SN7404N	14	7	HEX INVERTER
8	N7451A	14	7	2-IN AND/OR INV GATE
13, 16	N8885A	14	7	QUAD 2-INPUT NOR
15	N8875A	14	7	TRIPLE 3-INPUT NOR
18	N8281A/DC	14	7	4 BIT BINARY COUNTER
20	N8241A	14	7	QUAD 2-IN EXCLUSIVE OR
21	N8870A	14	8	TRIPLE 3-INPUT NAND
22	AM93L66	16	8	4 BIT UP/DOWN COUNTER
9	SN74HC01N	14	7	QUAD 2 INPUT NAND

3. CUT JUMPER FOR CONTINUOUS REAL TIME NUMERIC DISPLAY.
2. RESISTORS ARE IN OHMS, 1/4 W, 5%.
1. CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ±	FRAC ±
2 PL DEC ±	ANGLES ±

Princeton Applied Research Corporation
Princeton New Jersey

TITLE

CONTROL CARD SCHEMATIC XII-23

SCALE

DATE 2-9-72
5-11-72

DWG NO. 111527

LETTER	REVISION	DATE	DRAWN	CHKD	APPD
A	REDRAWN WITH CHANGES	JUNE 12-72			
B	ADDED SWITCHES S1 AND S2.	9.22.72			
C	ADDED NOTE 3 I.C. 6 WAS N7474N	JAN 7-73			

CONNECTIONS FOR S1 AND S2			
S1		S2	
NORMAL	REVERSE	NORMAL	REVERSE
A9 TO A10	A9 TO A12	A7 TO A8	A7 TO A6
A11 TO A12	A11 TO A10	A5 TO A6	A5 TO A8
SPARE	SPARE	A3 TO A4	A3 TO A2
SPARE	SPARE	A1 TO A2	A1 TO A4

DELINHDI
HOLDDI
PRERESETDØ
SPARE
PRECOMPDI
RESET 2 S2
INPUT 2
OUTPUT 2 S1
RESET 1 S2
INPUT 1
OUTPUT 1 S1
FRBLANKDI
PRESW16BI
DELSW16BI
PGMPRE16BI
PREP6MDØ
SDELAYDØ
DELBLANK20Ø
DELBLANKDI
PRECLOCK20Ø
ACOMP RØ R1 R2 R3 BCOMP
AØ A1 A2 A3 BØ B1 B2 B3
Vcc
R1 200
R2 1K
R3 1K
R4 3K
R5 3K
R6 1K
R7 1K
R8 3K
J901 FROM PRESET/DELAY SWITCH
+5V
GROUND
C1 22 15V
C2 0.1 100V
C3 0.1 100V
C4 0.1 100V
C5 0.1 100V
C6 0.1 100V

NOTES: EXCEPT AS NOTED
1. CAPACITORS ARE IN MICROFARADS.
2. RESISTORS ARE IN OHMS 1/4W 5%.
3. * DENOTES OPEN COLLECTOR OUTPUT.

I. D.	PART NO.	Vcc	GND	TYPE
1	N7451A	14	7	2—IN AND/OR INV GATE
2, 5, 8, 11	N8292A	14	7	4 BIT BCD COUNTER
3, 4, 9, 10, 14	MC4021P	16	8	DUAL COMPARATOR
6	SN74LS74	14	7	DUAL 'D' TYPE FLIP FLOP
7	N8875A	14	7	TRIPLE 3—INPUT NOR
12, 15	N8880A	14	7	QUAD 2—INPUT NAND
13	N8293	14	7	4 BIT BINARY COUNTER

REQD | PART NO. | DESCRIPTION | ITEM
LIST OF MATERIALS

MATERIAL:
FINISH:
DRAWN
CHECKED
APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± | FRAC ±
2 PL DEC ± | ANGLES ±

Princeton Applied Research Corporation
Princeton, New Jersey

TITLE
PRESET CARD SCHEMATIC

SCALE
DATE 2-3-72
DWG NO. 111530 C

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	ADDED NOTE 3. I.C. 2 & 8 WERE N7474A I.C. 6 & 14 WERE N74192B	JAN 8-74			

FRBLANKDI FRRETRACEDØ INBLANKDI PREMARKDI CHMARKDI

ADDRESS REGISTER / CURSOR COUNTER

ADRØ1DI ADRØ2DI ADRØ4DI ADRØ8DI ADR1DI ADR2DI ADR4DI ADR8DI ADR2ØDI ADR22DI ADR24DI ADR28DI

IMHZDI +5V GROUND

CHMK24DI CHMK21DI CHMKØ4DI CHMKØ2DI PREMK24DI PREMK21DI PREMK11DI PREMKØ1DI 511DØ 110DØ

CHMK11DI CHMKØ2DI

ACOMP BCOMP CHMK24DI CHMK21DI PREMK24DI PREMK21DI CHMK11DI PREMK11DI CHMKØ4DI CHMKØ2DI PREMKØ1DI

R1 1K Vcc R2 1K Vcc R3 3K Vcc R4 3K Vcc

C1 22 15V C2 0.1 100V C3 0.1 100V C4 0.1 100V C5 0.1 100V C6 0.1 100V C7 0.1 100V C8 0.1 100V C9 0.1 100V

CKUP CKDWN AIN BIN CIN DIN CAR BOR FRRETRACEDI ENDDOWNDØ ENDUPDI FØ F1 F2 F3 SØ S1 AØ A1 A2 A3 BØ B1 B2 B3

SPARE

SØ	S1	F	MODE
Ø	Ø	B	Ø→499
Ø	1	B	N/A
1	Ø	A	NORM
1	1	Ø	499→Ø

N8233B

AUSTARTDØ

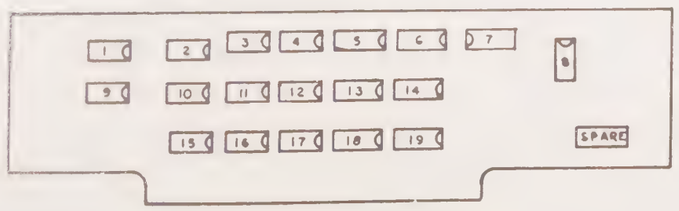
PREMARKCOUNTER PREMK12BI

CHMARKCOUNTER CHMK12BI

CURSOR COMPARATORS

PGMLNØ1DI PGMLNØ2DI PGMLNØ4DI PGMLNØ8DI PGMLN11DI PGMLN12DI PGMLN14DI PGMLN18DI PGMLN21DI PGMLN22DI PGMLN24DI PGMLN28DI

CURSUPDØ CURSDWNDØ LNZERODØ LNSTROBEDØ



I.D.	PART NO.	Vcc	GND	TYPE
1	N7408A	14	7	QUAD 2-INPUT AND
9	N7474A	14	7	DUAL 'D' TYPE FLIP FLOP
3,4,11,12,16,17	N8280A/DC	14	7	4 BIT BCD COUNTER
5,13,18	MC4021P	16	8	DUAL COMPARATOR
19	N74192B	16	8	4 BIT UP/DOWN COUNTER
7	N8233B	16	8	2 IN 4 BIT MULTIPLEXER
10	N8816A	14	7	DUAL 4-INPUT NAND
15	N8880A	14	7	QUAD 2-INPUT NAND
2,8	SN74LS74N	14	7	DUAL 'D' TYPE FLIP FLOP
6,14	AM93L60	16	8	4 BIT UP/DOWN DECADE

3. * DENOTES OPEN COLLECTOR OUTPUT.
2. RESISTORS ARE IN OHMS, 1/4W, 5%.
1. CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± FRAC ±

2 PL DEC ± ANGLES ±

Princeton Applied Research Corporation
Princeton New Jersey

TITLE

CURSOR CARD SCHEMATIC XII-25

SCALE

DATE 1-28-72

DWG NO. 111532 A

LETTER	REVISION	DATE	DRWN	CHKD	APR
C	U1 WAS N74S74A. 24,52,73				
B	I.C. 3,6,8,10,16,17 WERE N74174A I.C. 1, 19-26 WERE N74192B	JAN 8-74			

2MHZDI INTSWDØ INTDI

INTRDØ

IRDOWNDØ

BDI

ADØ

RUNDI

INTXIØSWDØ

Vcc

R1 2K

Σ X 100 MODE DIVIDER

CUPDI
IRNEGDI

ADØ

BDI

CKUP

CKDOWN

CAR

BOR

ORUPDØ

ORDOWNDØ

RESETORDI

ORT2DØ

ORBORROWDØ

INTRDØ

CUPDI

INTRDØ

CDI

DIRECTION CHANGE FF

INTDI

RUNDI

IRBORROWDØ

INTSWDØ

ARITHMEGDI (14)

DIGNEGDI (E)

CURSOWNDØ (29)

CURSUPDØ (28)

CHMARKDI (27)

SPARES

AUCLOCKDØ (F)

INTDI

INTERRORDØ (32)

IRNEGDI

ORCARRYDØ

T5BI — TØDI (5), T1DI (6), T2DI (7), T3DI (8), T4DI (9)

EMORDI (20)

C4BI — CØ1DI (10), CØ2DI (11), CØ4DI (12), CØ8DI (13)

ORDOWNDØ

ORUPDØ

RESETORDI

INTEGRATE REGISTER (IC 23-26)

IRBORROWDØ

IRDOWNDØ

ORBORROWDØ

ORCARRYDØ

Vcc

C1 0.1 100V, C2 0.1 100V, C3 0.1 100V, C4 0.1 100V, C5 0.1 100V, C6 0.1 100V

C7 22 15V

+5V (2), (B)

GROUND (1), (A), (Y)

ORTØDØ (15)

ORT2DØ (16)

ORT4DØ (26)

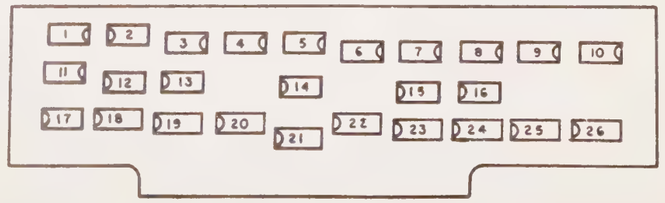
DIG2ØBI — DIGØ1DI, DIGØ2DI, DIGØ4DI, DIGØ8DI, DIG11DI, DIG12DI, DIG14DI, DIG18DI, DIG21DI, DIG22DI, DIG24DI, DIG28DI, DIG31DI, DIG32DI, DIG34DI, DIG38DI, DIG41DI, DIG42DI, DIG44DI, DIG48DI

DIGITAL OUTPUT REGISTER

2. RESISTORS ARE OHMS, 1/4W, 5%.

1, CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED



I.D.	PART NO.	Vcc	GND	TYPE
18	N74192B	16	8	4 BIT UP/DOWN COUNTER
2	N8870A	14	7	TRIPLE 3-INPUT NAND
5	N7474A	14	7	DUAL 'D' TYPE FLIP FLOP
4,7,11,14 15	N8880A	14	7	QUAD 2-INPUT NAND
9	N8885A	14	7	QUAD 2-INPUT NOR
12	N7404N	14	7	HEX INVERTER
13	N8241A	14	7	QUAD EXCLUSIVE OR
3,6,8,10,16,17	SN74LS74N	14	7	DUAL 'D' TYPE FLIP FLOP
1, 19-26	AM92L60	16	6	4 BIT UP/DOWN COUNTER

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

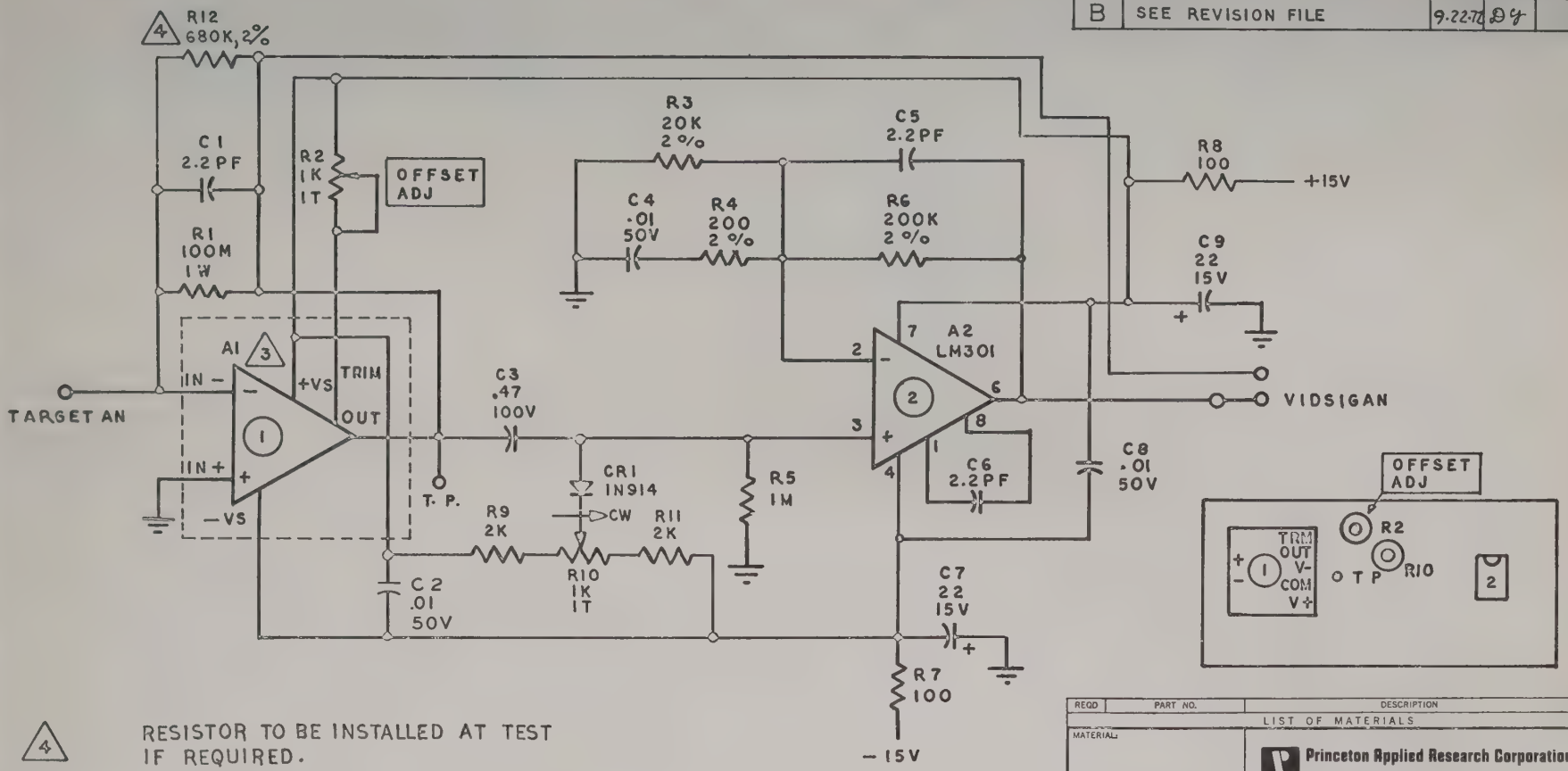
TITLE

INTEGRATE CARD SCHEMATIC

SCALE | DWG NO. 111529

DATE 1-27-72
5-15-72

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	JUNE 14-72	Gm	RK	
B	SEE REVISION FILE	9.22.72	DY		YBM



4 RESISTOR TO BE INSTALLED AT TEST IF REQUIRED.

3 ZELTEX ZA 804 MI.

2 RESISTORS ARE IN OHMS, 1/4W, 5%.

1 CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM

LIST OF MATERIALS

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

Princeton Applied Research Corporation
Princeton New Jersey

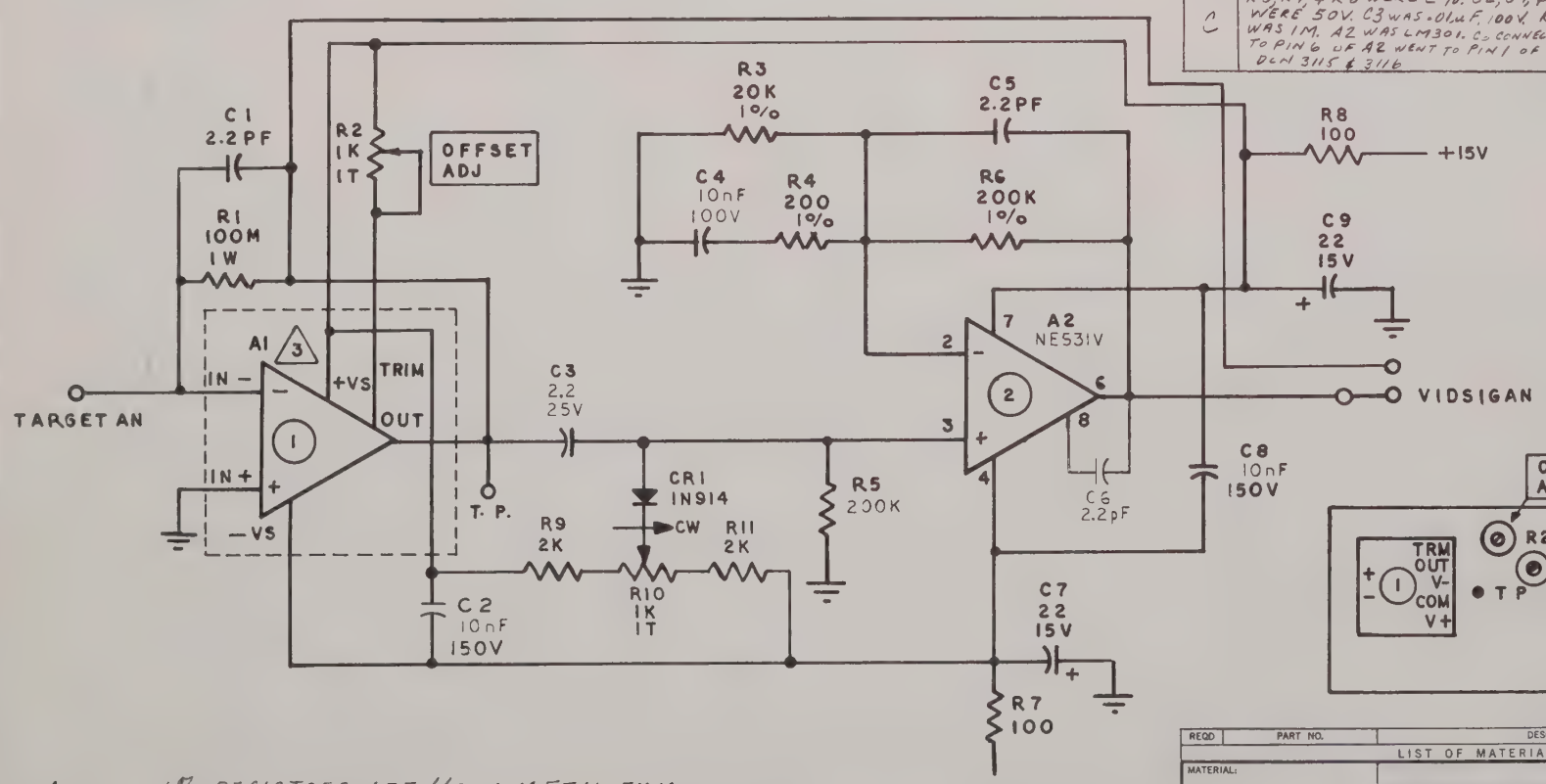
TITLE

VIDICON PREAMP BOARD SCHEMATIC

SCALE | DWG NO. 111723 | B

DATE 6-20-72

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	JUNE 14-72			
B	SEE REVISION FILE	9-22-72			
C	R3, R4 & R6 WERE 2%. C2, C4 & C8 WERE 50V. C3 WAS .01uF, 100V. R5 WAS 1M. A2 WAS LM301. C5 CONNECTION TO PIN 6 OF A2 WENT TO PIN 1 OF A2. DCN 3115 & 3116	11-19-74	FJB	FJB	



4 1% RESISTORS ARE 1/8 W METAL FILM.

3 ZELTEX ZA 804 MI.

2 RESISTORS ARE IN OHMS, 1/4W, 5%.

1 CAPACITORS ARE IN MICROFARADS.

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM

LIST OF MATERIALS

MATERIAL:

FINISH:

DRAWN

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

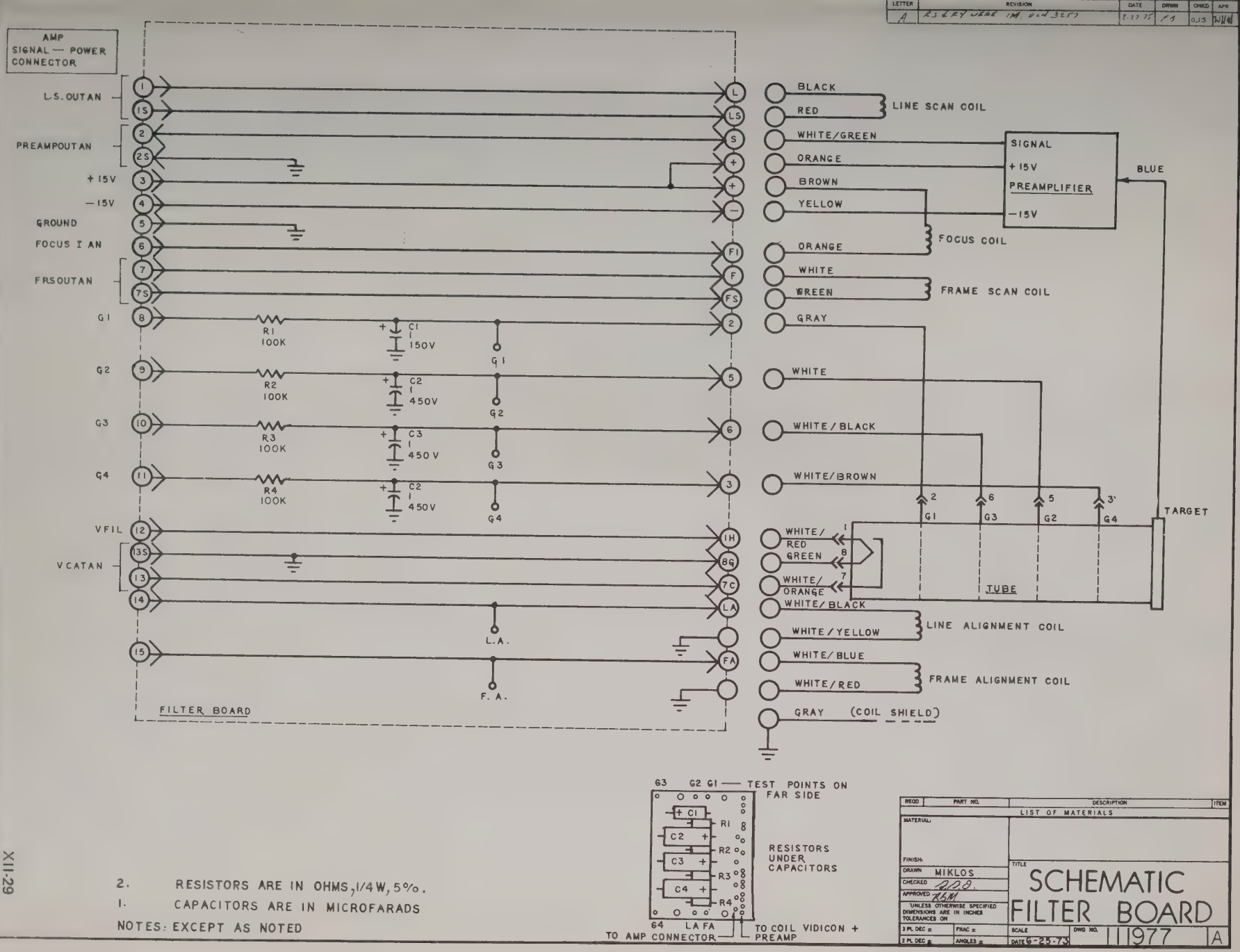
Princeton Applied Research Corporation
Princeton, New Jersey

TITLE

VIDICON PREAMP BOARD SCHEMATIC

SCALE | DWG NO. 111723 C

DATE 4-28-72



LETTER	REVISION	DATE	DRWN	CHKD	APR
A	R3 & R4 WERE 1M OHM 3-27-75				

2. RESISTORS ARE IN OHMS, 1/4W, 5%.
1. CAPACITORS ARE IN MICROFARADS

NOTES: EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL
FINISH
DRAWN MIKLOS
CHECKED
APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±
2 PL DEC ± ANGLES ±

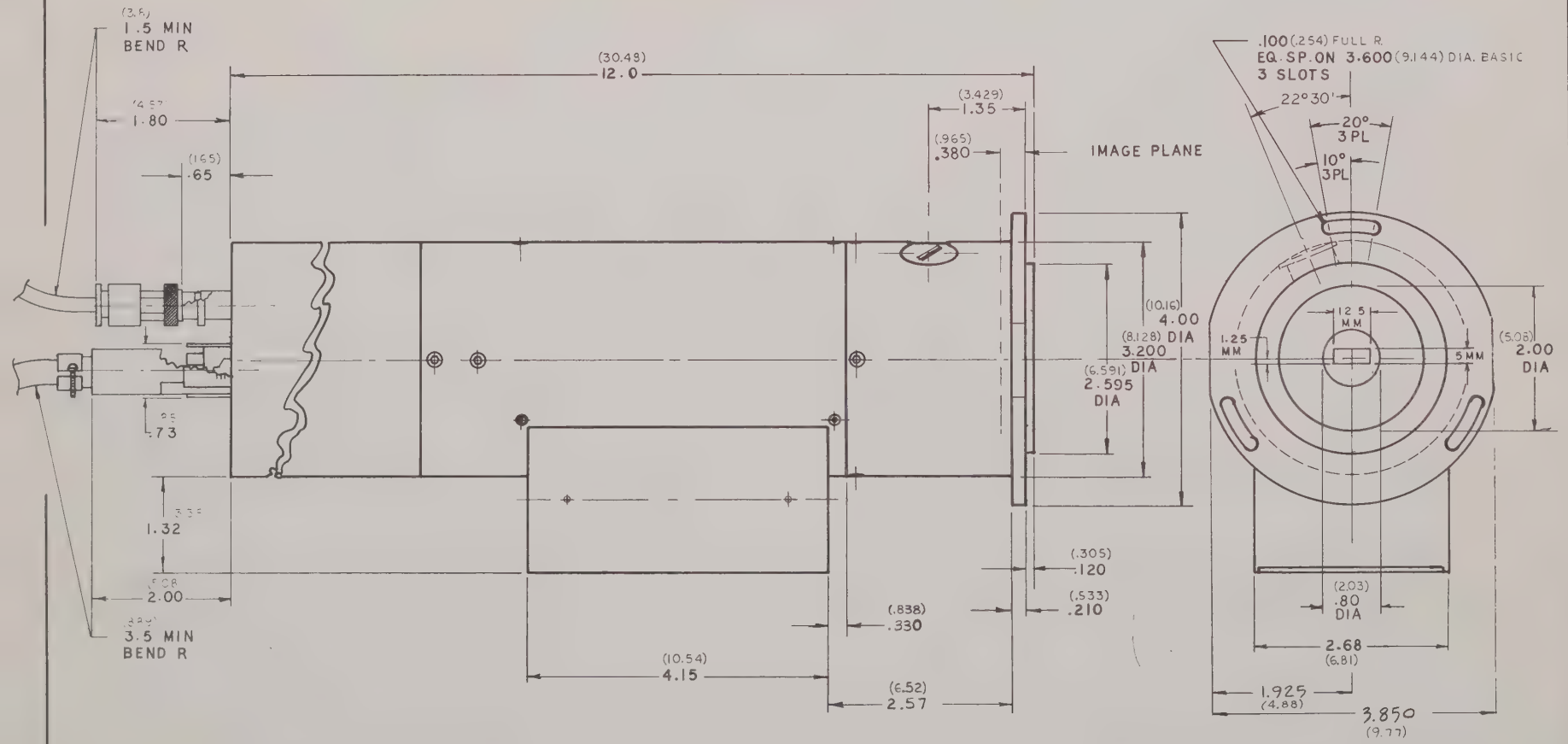
TITLE
SCHEMATIC FILTER BOARD

SCALE DWG NO. 11977 A
DATE 6-25-75

XII-29

LETTER	REVISION	DATE	DRWN	CHKD	APR
A	DIM .380 WAS .330	8-3-73	Dwg.		
B	ADDED NOTE 1 & ASSOCIATED CENTIMETER DIMENSIONS	1-28-75	FB		
C	ADDED FLATS ON FRONT CAP. & TWO HOLES ON HOUSING PRE-AMP. PCN 3239	3-4-75	DML	MS	MS

XII-30



REQD	PART NO.	DESCRIPTION	ITEM

LIST OF MATERIALS

MATERIAL

FINISH

DRAWN MIKLOS

CHECKED

APPROVED RBM 1/28/75

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

Princeton Applied Research Corporation
Princeton New Jersey

TITLE

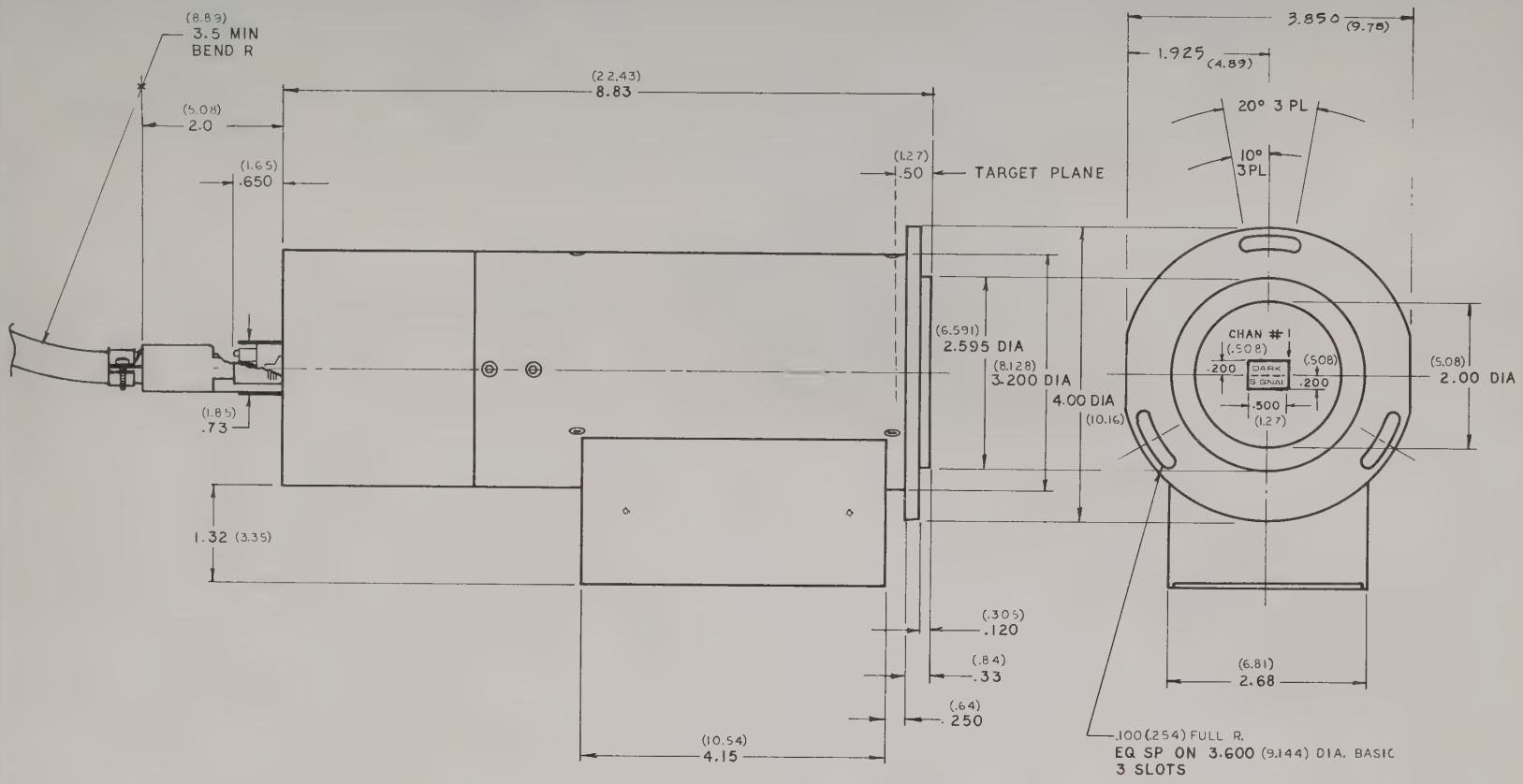
INTERFACE CONTROL DRAWING – 1205D

SCALE FULL | DWG NO. 10049 | C

1. DIMENSIONS IN PARENTHESIS ARE IN CENTIMETERS.

NOTES: EXCEPT AS NOTED

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	ADDED NOTE 1 & ASSOCIATED CENTIMETER DIMENSIONS	1-28-75	FB	[illegible]	[illegible]
B	ADDED DIMS 3.850 & 1.925, ALSO (2) 2-56-UNC HOLES PER DCN 3339	5-30-75	DML	[illegible]	[illegible]



1. DIMENSIONS IN PARENTHESIS ARE IN CENTIMETERS.

NOTES EXCEPT AS NOTED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN [signature]

CHECKED

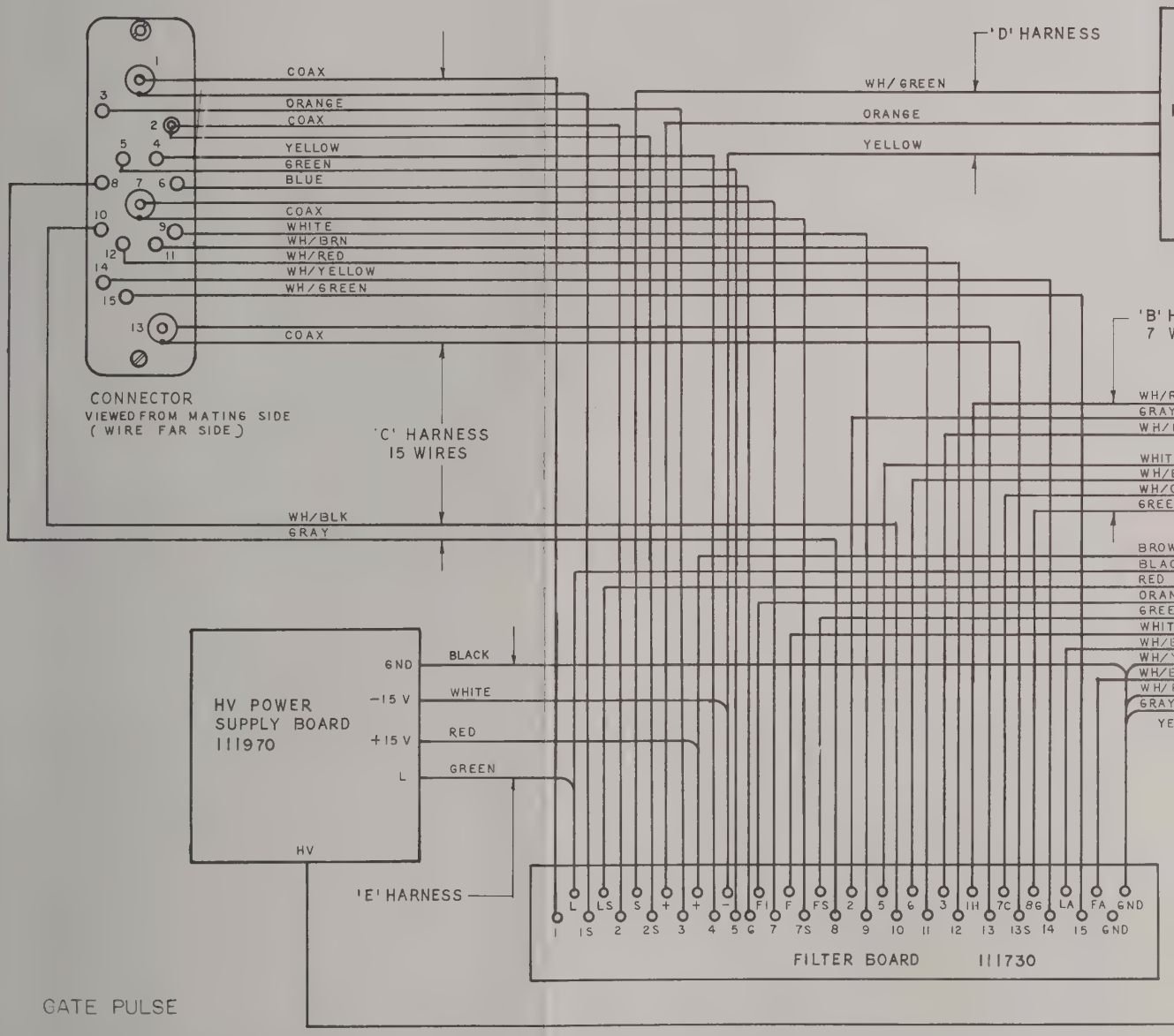
APPROVED [signature]

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
3 PL DEC ± FRAC ±
2 PL DEC ± ANGLES ±

Princeton Applied Research Corporation
Princeton New Jersey

TITLE
INTERFACE CONTROL
DWG – 1205B

SCALE FULL
DATE 2-17-73
DWG NO. 110048 B



5. PRIOR TO INSTALLING REMOVE TARGET CONTACT RING.

4. FOR WIRING OF HARNESS USE WIRING DIAGRAM.

3. PRELIMINARY COIL ALIGNMENT WITH LEAD BREAK OUT AT LOCATION SHOWN.

2. TIGHTEN SET SCREWS TO MAKE. CONTACT TO TUBE.

1. TIGHTEN LOCK RING FINGER TIGHT, AFTER INSTALLING TUBE.

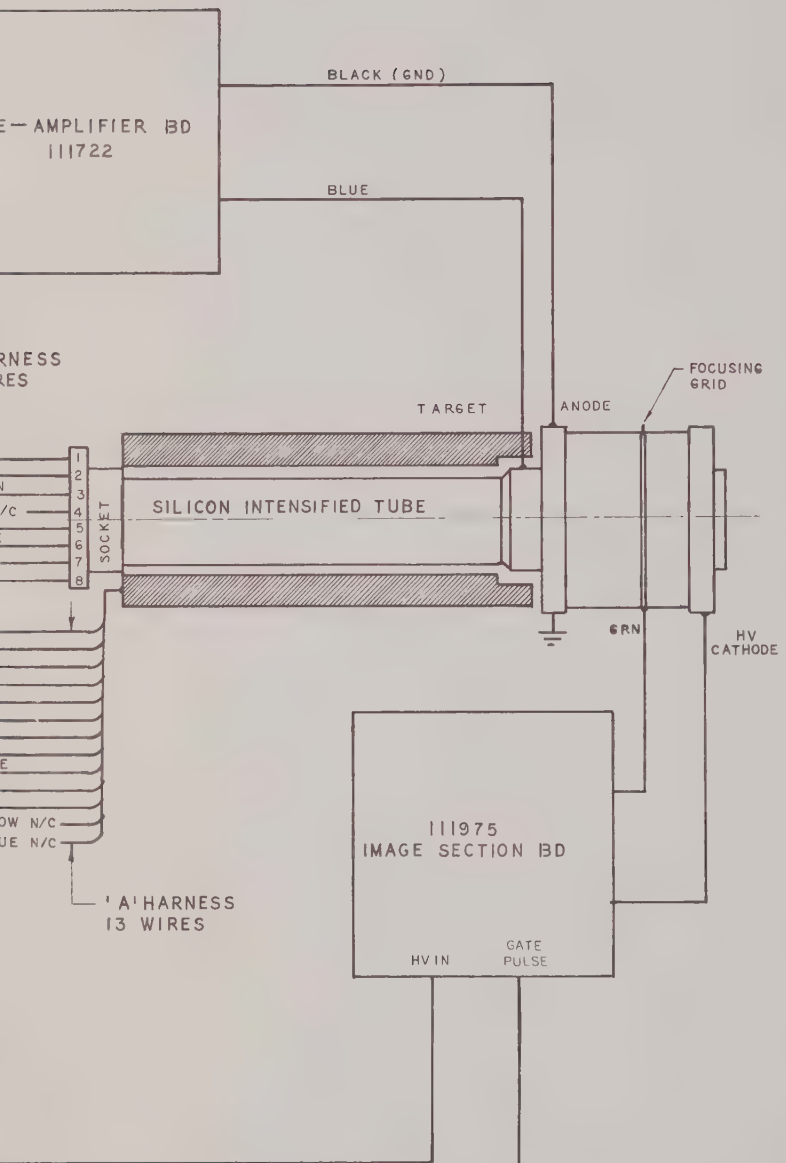
NOTES: EXCEPT AS NOTED

WIRING DIAGRAM

7. SHOWN: NORMAL POSITION
OPPOSITE GATED POSITION

6. BOND PLASTIC INSULATOR IN FRONT CAP ASSEMBLY USING THE PLUG FOR ALIGNMENT. LEAVE PLUG ON AND CURE.

LETTER	REVISION	DATE	DRWN	CHKD	APP'D
A	ITEM 25 WAS 201330-1	JAN 22-74			
B	ADDED ITEM 12, 43 & 44, ITEM 2 WAS 111195, TITLE WAS POSITIVE, REVISED SHT 2 TO AGREE WITH NEW DESIGN PER DCN 3239	3/3/75	DML		



REQD	PART NO.	DESCRIPTION	ITEM
1	2504-0058	RING, GASKET RUBBER	45
3	2811-0026	SCR, MACH, PAN HD 4-40 x 1/2	44
1	2504-0057	O RING BUNA-N, PARKER 2-231	43
4	2514	WASHER, PLASTIC NO.4, .06 THK; H.H. SMITH	42
6	6-32 X 3/8 LG	SCREW, MACH; ST-S-BK-HSO	41
1	4-40 X 1/2 LG	SCREW, MACH; BI-S-C-PH	40
16	4-40 X 3/8 LG	SCREW, MACH; BI-S-C-PH	39
4	4-40 X 3/8 LG	SCREW, MACH; SO-S-BK-HSO	38
4	4-40 X 1/4 LG	SCREW, MACH; SO-S-BK-HSO	37
1	4-40 X 5/8 LG	SCREW, MACH; FT-S-C-PH	36
10	4-40 X 1/4 LG	SCREW, MACH; FT-S-BK-HSO	35
8	8403	SPACER, 4-40 X 1/4 O.D. X 1/2 LG; H.H. SMITH	34
2	3-56 X 3/8 LG	SCREW, MACH; BI-S-C-PH	33
1	201924-1	SET, LOCKING SPRING AMP	32
3	201142-2	SPRING, RETENTION	31
1	200389-4	PIN, GUIDE, FEMALE	30
1	200390-4	PIN, GUIDE, MALE	29
1	201785-4	HOOD, PIN	28
3	328666	FERRULE, ORANGE	27
1	1-332056-0	FERRULE	26
11	201578-1	CONTACT, PIN, TYPE II	25
3	201144-1	CONTACT, SOCKET COAXICON	24
1	51561-1	CONTACT, PIN, SUB-MIN, COAX; AMP	23
1	201597-1	BLOCK, MALE HOUSING	22
			21
1	SF48	COVER, PLASTIC; CAPLUGS	20
1	111956	TUBE; RCA (4804)	19
1	ZA804MI	OP-AMP; ZELTEX	18
1	1465	COIL; PENTRAN	17
AR	# 24	WIRE, COLOR AND LENGTH AS REQD	16
			15
1	111965	ASSY, IMAGE SECTION	14
1	111970	ASSY, HV POWER SUPPLY BD	13
1	111968	INSULATOR, OUTER CYLINDER	12
1	111980	PLUG, FRONT CAP	11
1	110022	TAG, HV CAUTION	10
1	111964	HOUSING, ASSEMBLY,	9
2	111962	SUPPORT, CONNECTOR PLATE	8
1	111961	PLATE, CONNECTOR	7
1	111960	CAP, REAR	6
1	111963	ASSY, FRONT CAP	5
1	111730	ASSY, FILTER BOARD	4
1	111722	ASSY, PRE/AMPLIFIER BOARD	3
1	9454-A-MD	NAMEPLATE (2515-0271-06)	2
1	110502-2	CONNECTOR, MHV	1

LIST OF MATERIALS

MATERIAL:

FINISH:

DRAWN M.C.L. 6/5

CHECKED

APPROVED R.B. Mikulski

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

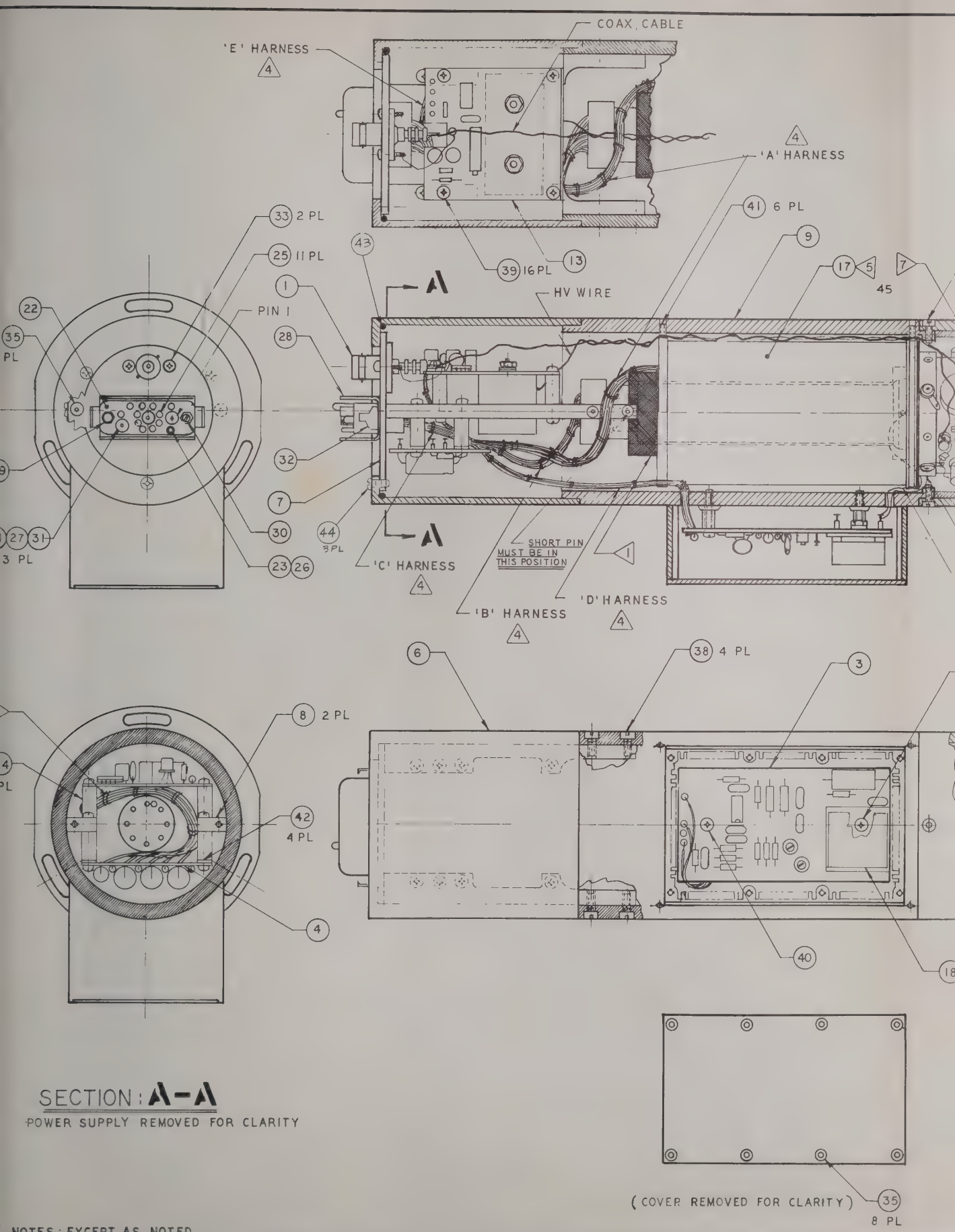
Princeton Applied Research Corporation
Princeton New Jersey

TITLE

SIT, ASSEMBLY
M7054

SCALE FULL | DWG NO. 111950 | SHT 1 OF 2 | B

DATE 6-5-73



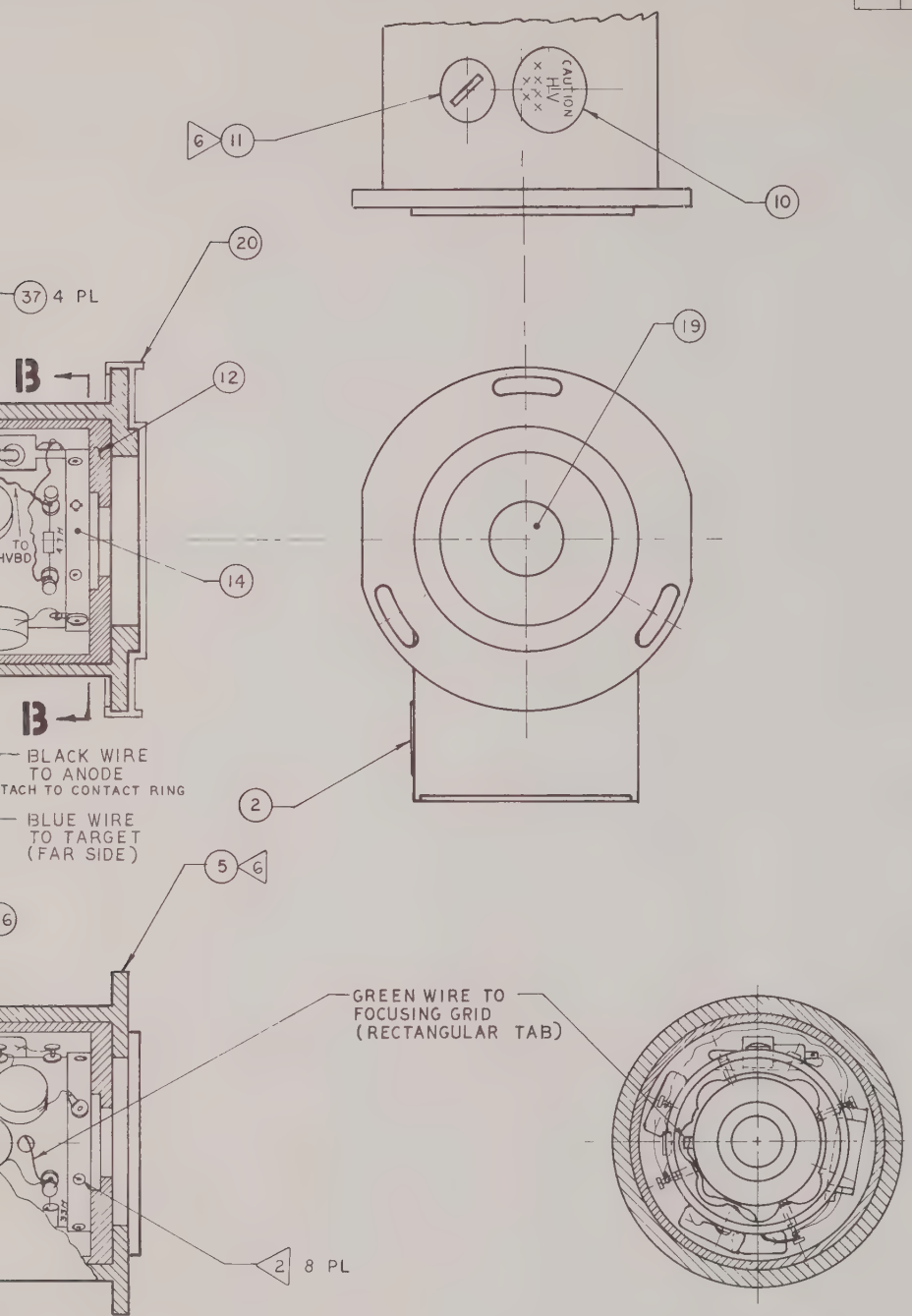
SECTION : A-A

POWER SUPPLY REMOVED FOR CLARITY

NOTES : EXCEPT AS NOTED

LETTER	REVISION	DATE	DRWN	CHKD	APR.
	SEE REVISION FILE	JAN 22-74			

SEE SHT 1 FOR LATEST REVISIONS



SECTION: B-B

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN Mitchell

CHECKED

APPROVED T. E. Mitchell

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

Princeton Applied Research Corporation
Princeton, New Jersey

TITLE

SIT, ASSEMBLY

XII-33

M7054

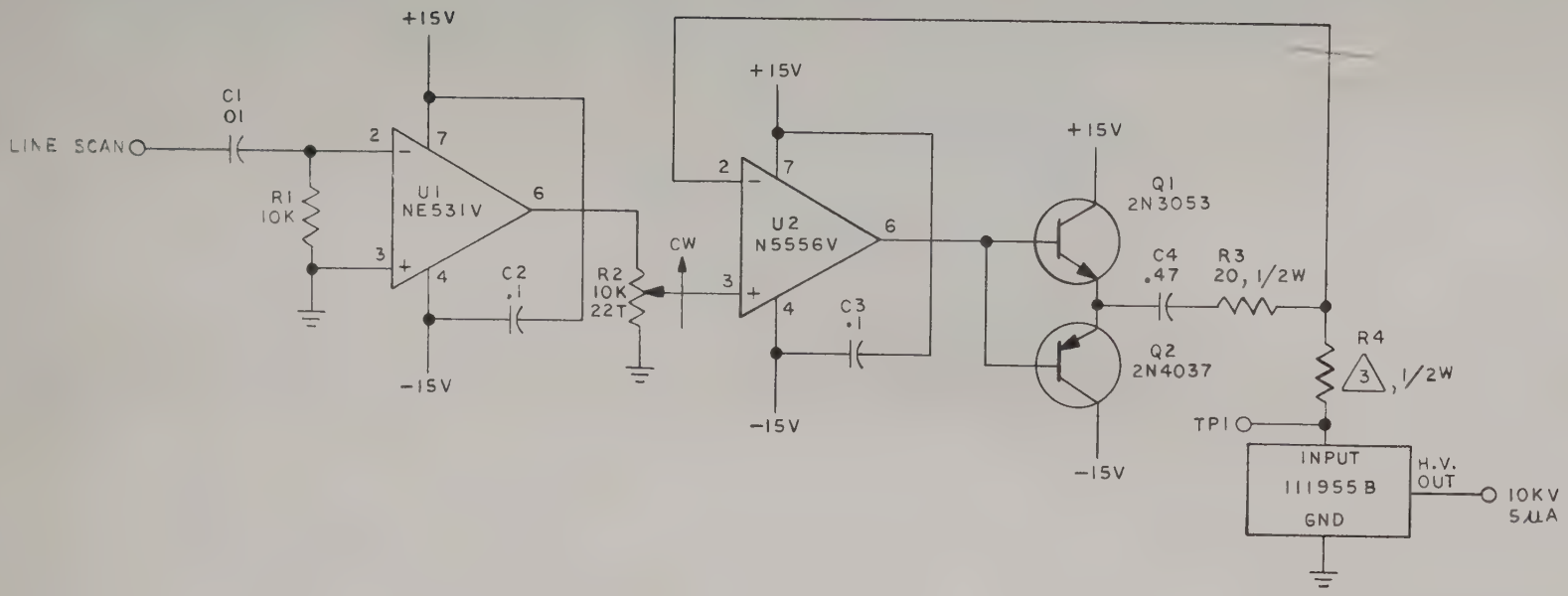
SCALE FULL

DWG NO. 111950

SHT 2 OF 2

DATE 6-5-73

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REVISED AND REDRAWN	9-27-73	D.Y.		



3 SELECT FOR PROPER FULL SCALE VOLTAGE, INSTALL AT TEST.

2. CAPACITORS ARE IN MICROFARADS, 100V.

1. RESISTORS ARE IN OHMS ±5%, 1/4W.

NOTES-UNLESS OTHERWISE SPECIFIED

REQD	PART NO.	DESCRIPTION	ITEM
		LIST OF MATERIALS	

MATERIAL:

FINISH:

DRAWN Dye

CHECKED

APPROVED RBM

'UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ±	FRAC ±
2 PL DEC ±	ANGLES ±

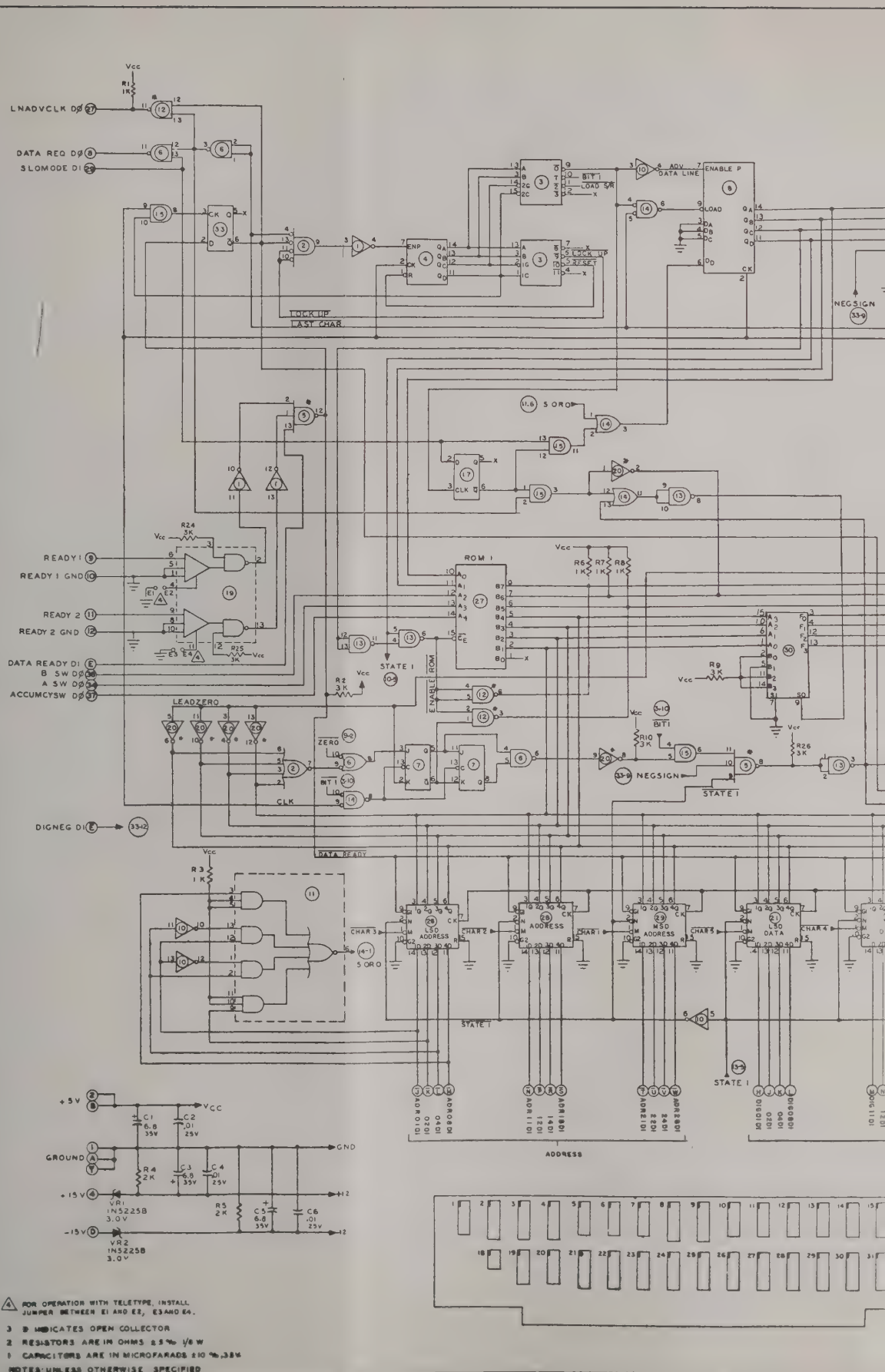
Princeton Applied Research Corporation
Princeton, New Jersey

TITLE

H.V. POWER SUPPLY SCHEMATIC DIAGRAM

SCALE NONE DWG NO. 111969 A

DATE 9-27-73



4 FOR OPERATION WITH TELETYPE, INSTALL JUMPER BETWEEN E1 AND E2, E3 AND E4.

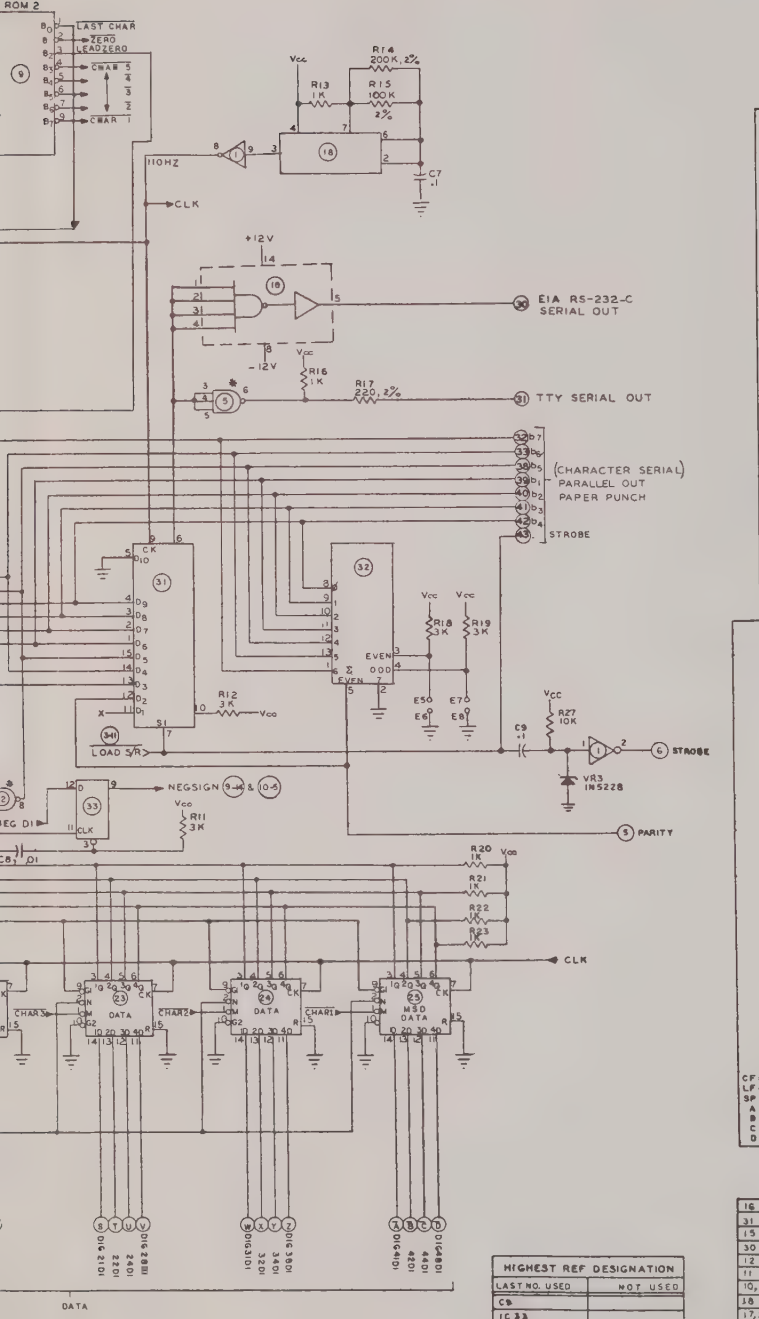
3 Ø INDICATES OPEN COLLECTOR

2 RESISTORS ARE IN OHMS ±5% 1/8 W

1 CAPACITORS ARE IN MICROFARADS ±10 %, 35V

NOTES: UNLESS OTHERWISE SPECIFIED

LETTER	REVISION	DATE	DRAWN	CHKD	APD
A	SEE REVISION FILE	11-12-73			



ROM 2

OUTPUT

ADDRESS

ADDRESS	STATE	OUTPUT
00000	STATE I	LEADZERO
00001		LEADZERO
00010		CHAR 1 DATA
00011		2
00100		3
00101		4
00110		CHAR 5 DATA
00111		LAST CHAR
01000		
01001		ROM 1
01010		WORKING
01011		
01100	STATE I	LEADZERO
01101		CHAR 1 ADDRESS
01110		2
01111		CHAR 3 ADDRESS
10000		LEADZERO
10001	STATE I	CHAR 1 DATA
10010		3
10011		4
10100		CHAR 5 DATA
10101		LEADZERO LAST CHAR
10110		LEADZERO LAST CHAR
10111		
11000		ROM 1
11001		WORKING
11010	STATE I	
11011		LEADZERO
11100		CHAR 1 ADDRESS
11101		2
11110		CHAR 3 ADDRESS
11111		

NEGSIGN

ROM 1

ADDRESS

ACCUMSW, ASWD0, BSWD0

OUTPUT

ADDRESS	OUTPUT	
00000	XXXXXXXX	NOT USED
00001	XXXXXXXX	
00010	XXXXXXXX	
00011	XXXXXXXX	
00100	00011010	CR
00101	00010010	LF
00110	10000001	A
00111	10000011	C
01000	00011010	CR
01001	00010010	LF
01010	10000010	B
01011	10000011	C
01100	00011010	CR
01101	00010010	LF
01110	10001000	D
01111	10000011	C
10000	XXXXXXXX	NOT USED
10001	XXXXXXXX	
10010	XXXXXXXX	
10011	XXXXXXXX	
10100	00011010	CR
10101	00010010	LF
10110	10000011	SP
10111	01000000	CR
11000	00011010	LF
11001	00010010	B
11010	10000010	SP
11011	01000000	CR
11100	00011010	LF
11101	00010010	D
11110	10001000	SP
11111	01000000	

CF = CARRIAGE RETURN
LF = LINE FEED
SP = SPACE
A = ASWD0 (A MEM)
B = BSWD0 (B MEM)
C = ACCUMCYSW D0
D = DIFFERENCE (A - B)

16	8T13	—	7	DUAL EIA RS-232 LINE DRIVER
31	8274	16	8	10 BIT PARALLEL IN SERIAL OUT SHIFT REG
15	7408	14	7	QUAD 2 INPUT POS AND
30	8233	16	8	2 INPUT 4 BIT MULTIPLEXER
12	74LS03	14	7	QUAD 2 INPUT NAND *
11	74LS54	14	7	4 WIDE 2 3 3 2 INPUT AND NOR GATE
10,1	74LS04	14	7	HEX INVERTER
38	NE555	8	1	TIMER
17,33	74LS74	14	7	DUAL D TYPE POS EDGE FLIP FLOP
14	7432	14	7	QUAD 2 INPUT OR
7	74LS114	14	7	DUAL J K NEG EDGE TRIG FLIP FLOP
6,13	74LS00	14	7	QUAD 2 INPUT NAND
2	7423	16	8	DUAL 4 INPUT NOR
4,8	74163	16	8	SYNCHRONOUS 4 BIT COUNTER
3	74LS155	16	8	DUAL 2 TO 4 LINE DECODERS
5	7412	14	7	TRIPLE 3 INPUT NAND GATES *

IDENTIFY	PART NO.	Vcc	GND	TYPE

LIST OF MATERIALS

HIGHEST REF DESIGNATION	
LAST NO. USED	NOT USED
C9	
IC 33	
R27	
VR3	

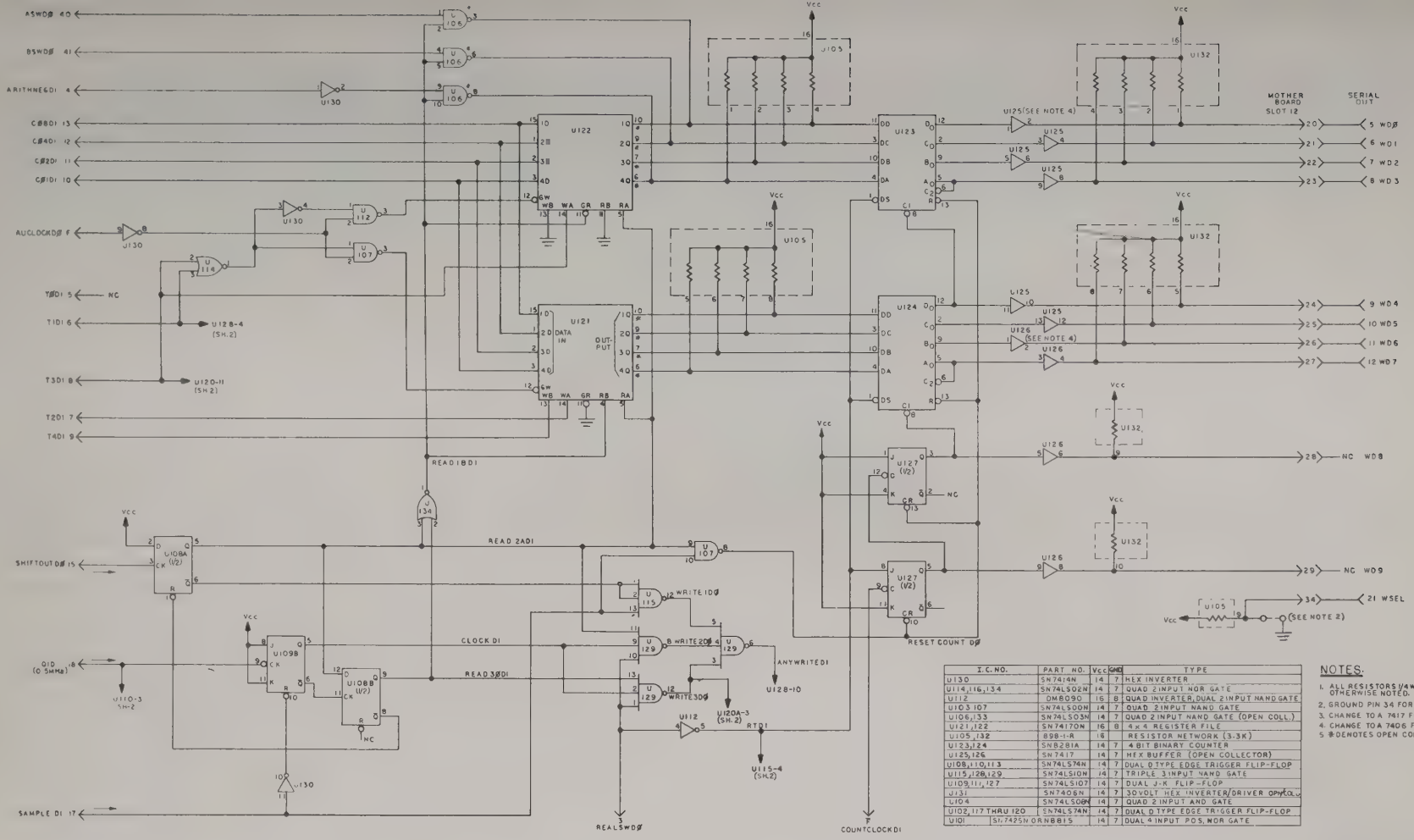
9	825123	16	8	256 (32 X 8) PROM TRI-STATE
22,23,24,25,26,28,29,21	8551 or 74173	16	8	4 BIT D TYPE F/F TRI-STATE OUTPUT
32	74180	14	7	8 BIT ODD/EVEN PARITY GENERATOR
20	74LS05	14	7	HEX INVERTER *
27	8223	16	8	256 (32X8) PROM
19	8T16	14	7	DUAL EIA RS-232 LINE RECEIVER

IDENTIFY	PART NO.	Vcc	GND	TYPE

LIST OF MATERIALS

MATERIAL

DRAWN	E R KOCH
TITLE	SCHEMATIC — SERIAL CONVERTER
SIZE	111623 A

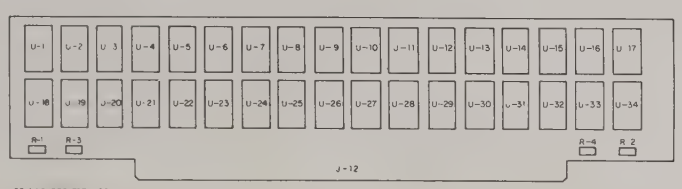


I.C. NO.	PART NO.	Vcc	GND	TYPE
U130	SN7414N	14	7	HEX INVERTER
U114,116,134	SN74LS02N	14	7	QUAD 2INPUT NOR GATE
U112	DM8090	15	8	QUAD INVERTER, DUAL 2INPUT NAND GATE
U103 107	SN74LS00N	14	7	QUAD 2INPUT NAND GATE
U106,133	SN74LS03N	14	7	QUAD 2INPUT NAND GATE (OPEN COLL.)
U121,122	SN74170N	16	8	4 x 4 REGISTER FILE
U105,132	898-1-R	16		RESISTOR NETWORK (3.3K)
U123,124	SN8281A	14	7	4 BIT BINARY COUNTER
U125,126	SN7417	14	7	HEX BUFFER (OPEN COLLECTOR)
U108,110,113	SN74LS74N	14	7	DUAL D TYPE EDGE TRIGGER FLIP-FLOP
U115,128,129	SN74LS10N	14	7	TRIPLE 3 INPUT NAND GATE
U109,111,127	SN74LS107	14	7	DUAL J-K FLIP-FLOP
U131	SN7406N	14	7	30VOLT HEX INVERTER/DRIVER OPN.CL.
U104	SN74LS08N	14	7	QUAD 2 INPUT AND GATE
U102,117 THRU 120	SN74LS74N	14	7	DUAL D TYPE EDGE TRIGGER FLIP-FLOP
U101	SI.7425 SN ORN8815	14	7	DUAL 4 INPUT POS. NOR GATE

NOTES:

1. ALL RESISTORS 1/4W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. GROUND PIN 34 FOR ZERO TRUE LOGIC.
3. CHANGE TO A 7417 FOR ZERO TRUE LOGIC.
4. CHANGE TO A 7406 FOR ZERO TRUE LOGIC.
5. * DENOTES OPEN COLLECTOR.

TAPE CONTROLLER W/AUTO CYCLE MODEL 1205-06A



30 AWG RED FOR VCC
32 AWG BLACK FOR GND

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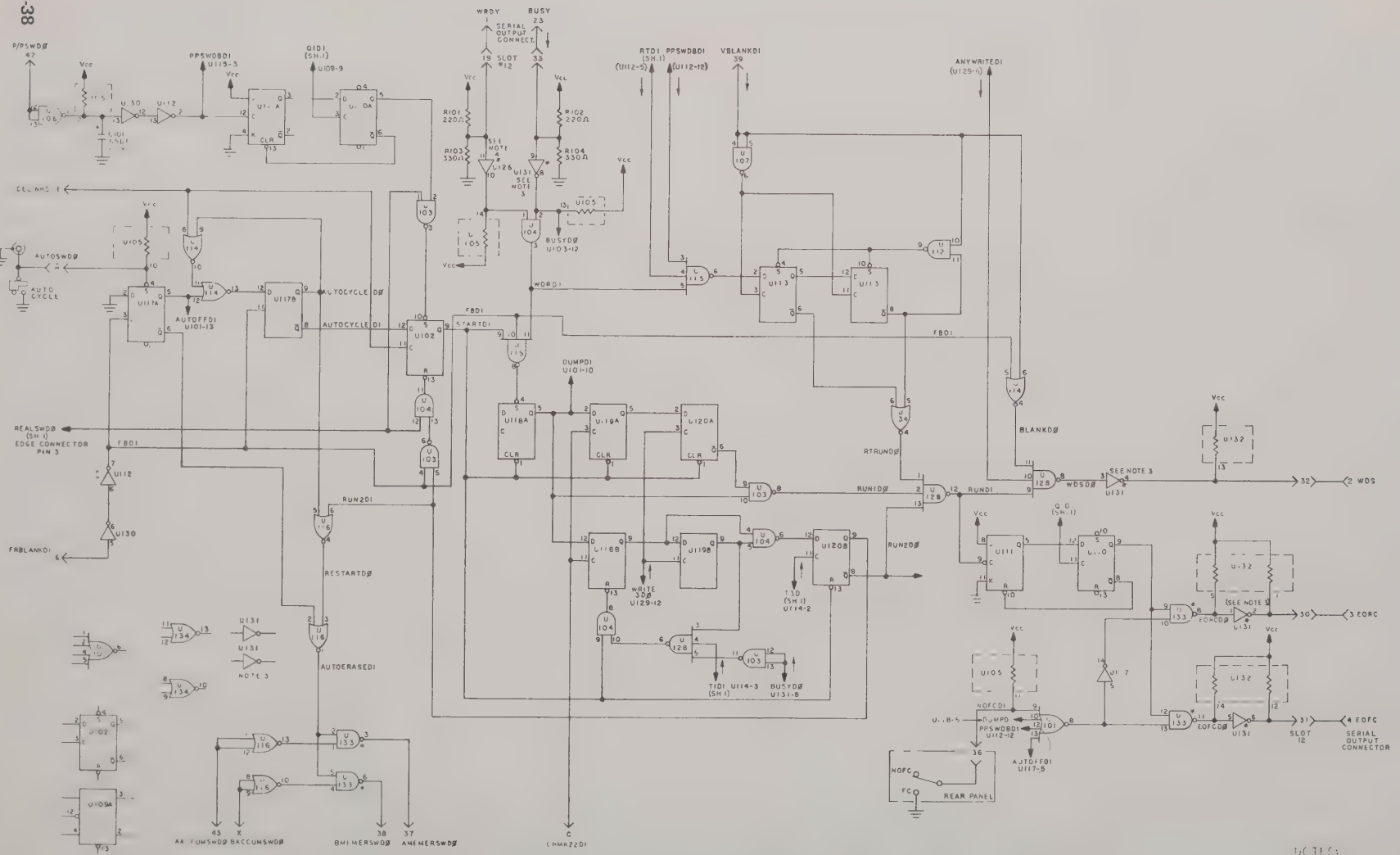
SHT 1 OF 2 111650 (1) SD A



NOTES:
SEE SHEET 1

TAPE CONTROLLER W/AUTO CYCLE

MODEL 1205-06A

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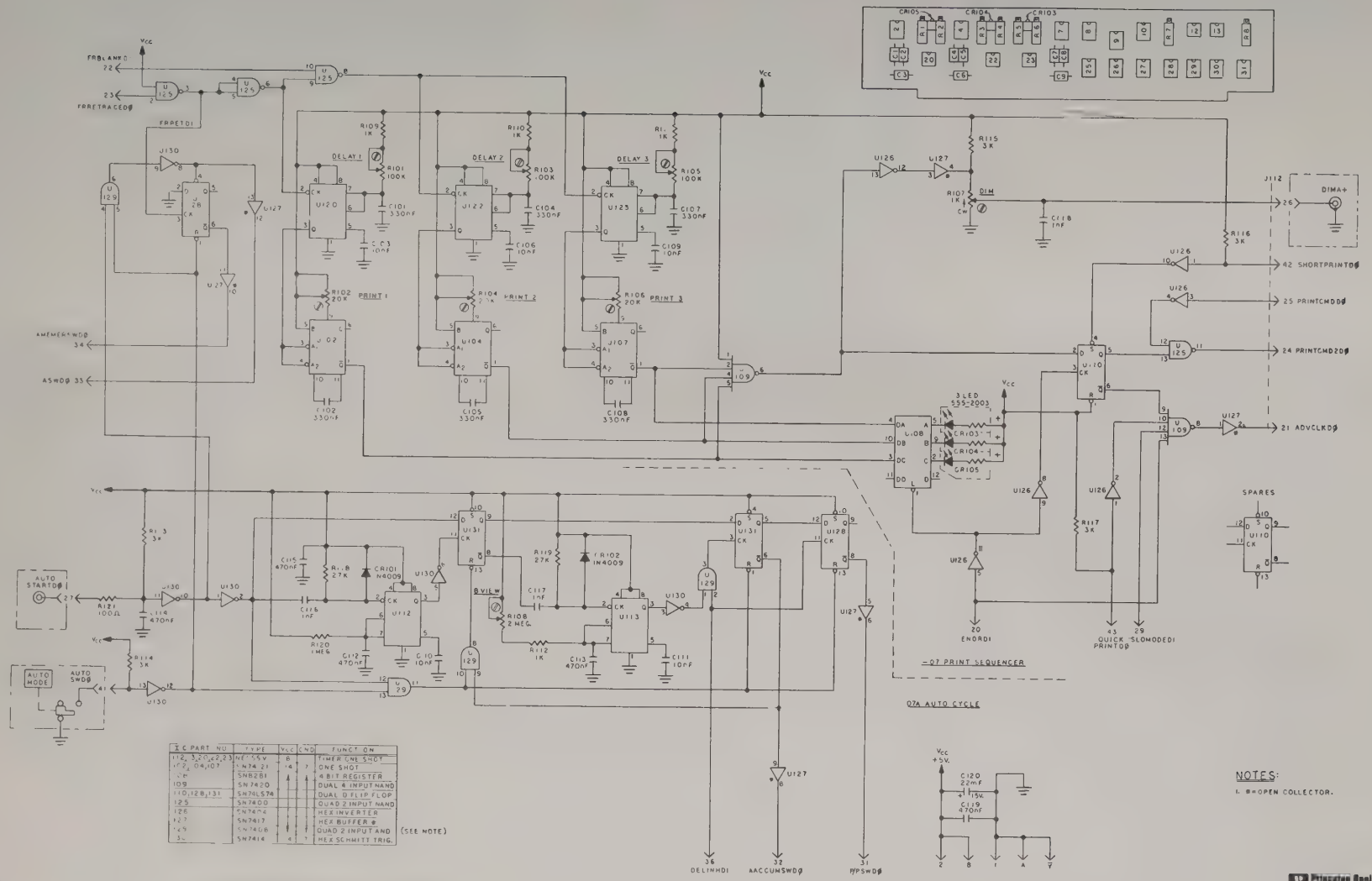

IC PART NO	TYPE	VCC	GND	FUNCTION
U112, 120, 122, 123	NE555V	8		TIMER ONE SHOT
U104, 107	SN7421	14	7	ONE SHOT
U102	SN8281			4 BIT REGISTER
U109	SN7420			DUAL 4 INPUT NAND
U110, 128, 131	SN74LS74			DUAL D FLIP FLOP
U125	SN7400			QUAD 2 INPUT NAND
U126	SN7404			HEX INVERTER
U127	SN7417			HEX BUFFER #
U129	SN7408			QUAD 2 INPUT AND
U130	SN7414	14	7	HEX SCHMITT TRIG.

(SEE NOTE)

NOTES:
1. #=OPEN COLLECTOR.

PRINT SEQUENCER CONTROLLER

MODEL 1205A-07A

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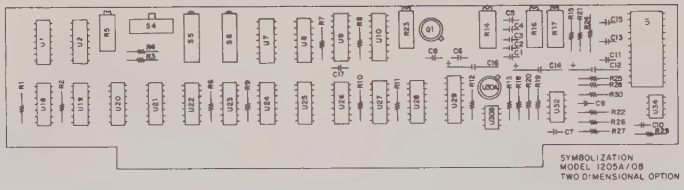
SHT. 1 OF 1 | 9083 | D | SD



SYMBOLIZATION
MODEL 1205A/08
TWO DIMENSIONAL OPTION 80

I D (L NO)	PART NO	Vcc	GND	TYPE
19,22	SN74LS02	14	7	QUAD 2 INPUT NOR
2	SN74LS196	14	7	DECADE COUNTER
9,10	MC4021P	16	8	DUAL COMPARATOR
7,8,25,26	SN74LS197	14	7	4 BIT BINARY COUNTER
1,23	SN74LS74N	14	7	DUAL D FLIP FLOP
18,20,21,24	SN74LS00	14	7	QUAD 2 INPUT NAND
27	AD7520LN			10 BIT D/A CONVERT.
30B	NE531V			OP. AMP.
32	LH0002CN			CURRENT AMP.
34	N5558V			DUAL OP. AMP.
30A	CA3100S			OP AMP
28	899-1-R3.3K	14		RESISTOR NETWORK
29	AD7520JN			10 BIT D/A CONVERTER

NOTES

1. ALL RESISTORS ¼W, 5%, CARBON COMP. EXCEPT AS NOTED.
2. J1 IS THE 24 PIN DIGITAL INTERFACE CONN.

1205A-08
TWO DIMENSIONAL OPTION

Princeton Applied Research Corporation
Post Office Box 2565, Princeton, New Jersey 08540

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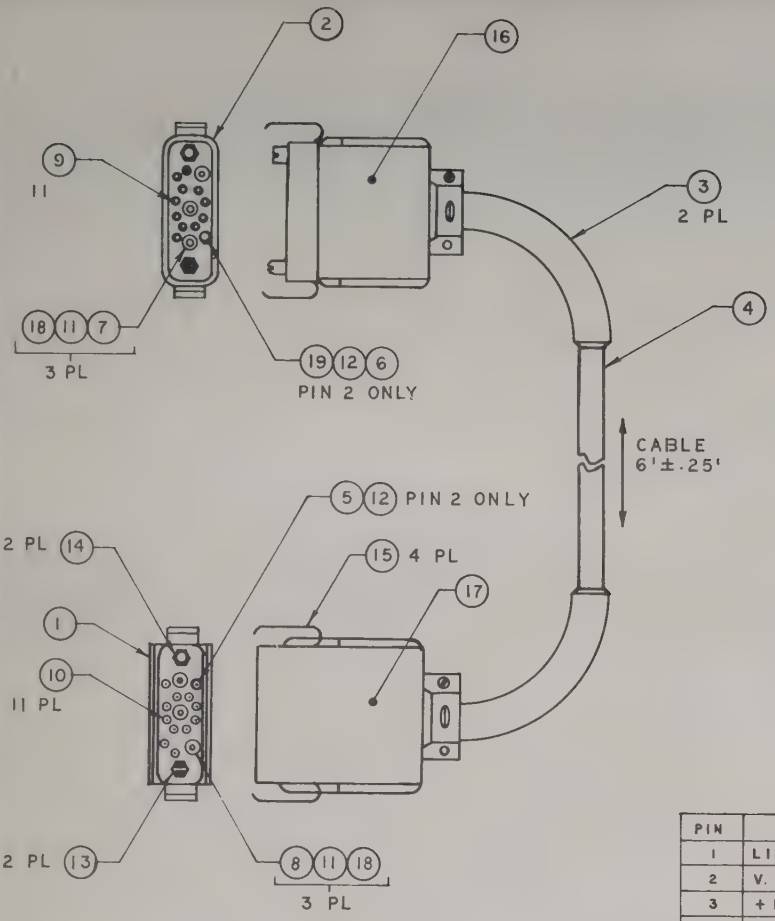
LETTER	REVISION	DATE	DRWN	CHKD	APD
A	ITEM 9 WAS 201328-1, ITEM 10 WAS 201330-1. ECN 3205	4-3	FB		



PIN	FUNCTION	WIRE COLOR
1	LINE SCAN	COAX YELLOW STRIPE
2	V. SIGNAL	COAX GREEN STRIPE
3	+15V	ORANGE
4	−15V	YELLOW
5	POWER GND	GREEN
6	FOCUS I	BLUE
7	FRAME SCAN	COAX, WHITE STRIPE
8	G1	GRAY
9	G2	WHITE
10	G3	BLACK−WHITE
11	G4	BROWN−WHITE
12	FILAMENT	RED
13	V CATHODE	COAX, PLAIN
14	LINE ALIGN	BROWN
15	FRAME ALIGN	VIOLET
SHELL	SHIELD GROUND	BRAIDED SHIELD

APPROVED FOR PROCUREMENT J.G. Hennes 5-1-72

PT NO. 6020-0328-16

REQD	PART NO.	DESCRIPTION	ITEM
			20
1	51609−1	SLEEVE A-MP	19
6	201142−2	SPRING, RETENTION,	18
1	201382−2	SHIELD, 180° PIN PROTECTION;	17
1	201169−2	SHIELD, 180° NON PROTECTED;	16
2	201923−1	SET LOCKING SPRING;	15
2	200390−4	PIN GUIDE, FEMALE;	14
2	200389−4	PIN GUIDE, MALE;	13
2	I−33205G−0	FERRULE	12
G	328666	FERRULE, ORANGE;	11
11	201578-1	CONTACT, PIN, TYPE II;	10
11	201580-1	CONTACT, SOCKET, TYPE II;	9
3	201144−1	CONTACT SOCKET COAXICON	8
3	201143−1	CONTACT, PIN, COAXICON	7
1	51565−1	CONTACT, SOCKET, SUBMIN, COAX.	6
1	51561−1	CONTACT, PIN, SUBMIN, COAX. A-MP	5
6'	111707	CABLE, SHIELDED, 16 COND ; ANY	4
2	9779−513−8 (AN3420−8)	BOOT, CABLE; AMPHENOL	3
1	201598−1	BLOCK, FEMALE HOUSING; A-MP	2
1	201597−1	BLOCK, MALE HOUSING; A−MP	1

LIST OF MATERIALS

MATERIAL:

FINISH:

DRAWN Lu Klop

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

PRINCETON APPLIED RESEARCH

TITLE

SIGNAL/POWER CABLE, 1205/AB

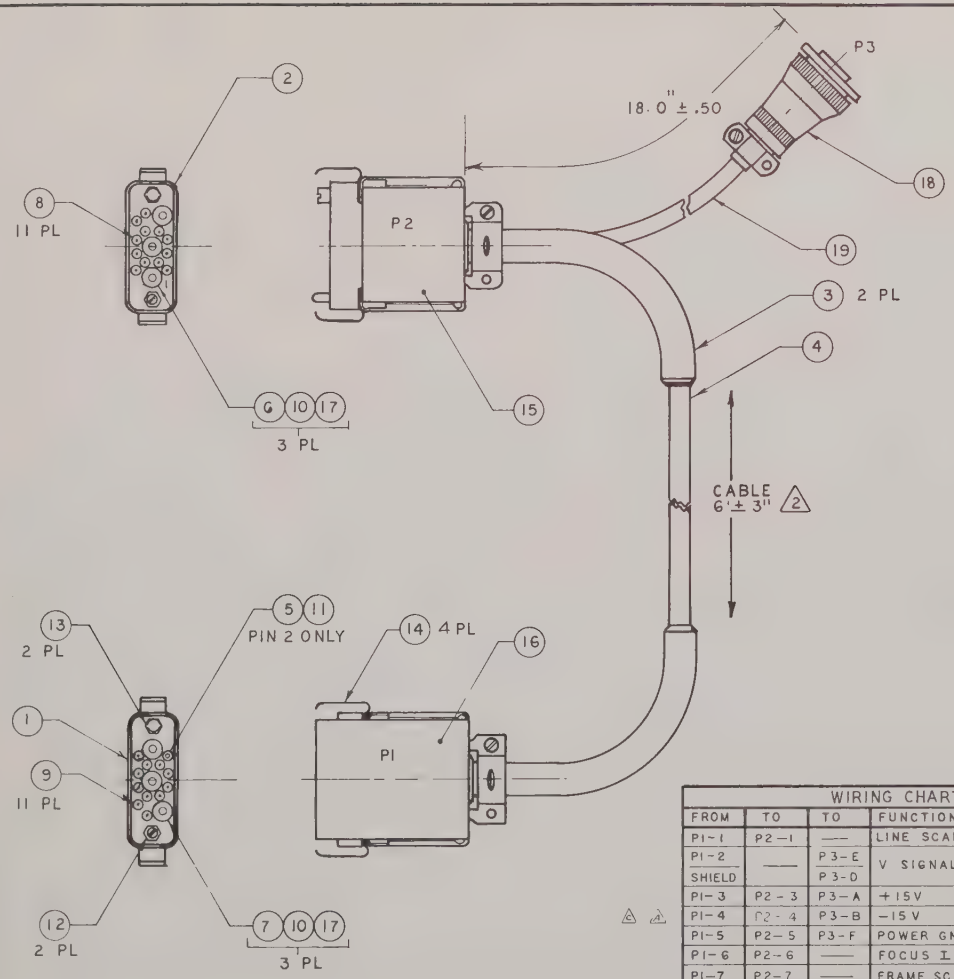
SCALE | DWG NO 110328 A

DATE 5-25-72

XII-141

1. ● MALE GUIDE PIN.
   ○ FEMALE GUIDE PIN.

NOTES: EXCEPT AS NOTED



WIRING CHART				
FROM	TO	TO	FUNCTION	WIRE COLOR
P1-1	P2-1	——	LINE SCAN	COAX YELLOW STRIPE
P1-2	——	P3-E	V SIGNAL	COAX GREEN STRIPE
SHIELD	——	P3-D		CENTER CONDUCTOR
P1-3	P2-3	P3-A	+15V	ORANGE (2 WIRES)
P1-4	P2-4	P3-B	-15V	YELLOW (2 WIRES)
P1-5	P2-5	P3-F	POWER GND	GREEN (2 WIRES)
P1-6	P2-6	——	FOCUS I	BLUE
P1-7	P2-7	——	FRAME SCAN	COAX WHITE STRIPE
P1-8	P2-8	——	G1	GRAY
P1-9	P2-9	——	G2	WHITE
P1-10	P2-10	——	G3	BLACK/WHITE
P1-11	P2-11	——	G4	BROWN/WHITE
P1-12	P2-12	——	FILAMENT	RED
P1-13	P2-13	——	V CATHOD	COAX, PLAIN
P1-14	P2-14	——	LINE ALIGN	BROWN
P1-15	P2-15	——	FRAME ALIGN	VIOLET
SHELL	SHELL	——	SHIELD GND	BRAIDED SHIELD
——	——	P3-C	N.C.	——

3. P1, P2 AND P3 REF DESIGNATIONS ARE FOR REF. ONLY.

△2 CUT CABLE 8 FT. STRIP BACK OUTSIDE JACKET 2 FT ON P2 END.

1 ⊛ DENOTES MALE GUIDE PIN.
○ DENOTES FEMALE GUIDE PIN.

NOTES UNLESS OTHERWISE SPECIFIED.

LETTER	REVISION	DATE	DRWN	CHKD	APR
A	ADDED CONN TO "P2-4". PER DCN 3127	12-11-74	DJS	[illegible]	[illegible]
B	ITEM 8 WAS 201328-1. DCN 3207	4-25-75	FA	[illegible]	[illegible]
C	ADDED YELLOW WIRE TO -15V, ITEM #14 QTY WAS 2 DCN 3396, 3417	5-30-75	DML	[illegible]	[illegible]

APPROVED FOR PROCUREMENT [signature] 2-17-75

PT. NO. 6020-0398-37

REQD	PART NO.	DESCRIPTION	ITEM
1	PVC #3	VINYL SLEEVING, BLACK	19
1	PCOGA-10-98S(SR)	CONNECTOR; BENDIX	18
6	201142-2	SPRING, RETENTION AMP	17
1	201382-2	SHIELD, 180°, PIN PROTECTION	16
1	201169-2	SHIELD, 180°, NON PROTECTED	15
4	201923-1	SPRING, LOCKING	14
2	200390-4	PIN GUIDE, FEMALE	13
2	200389-4	PIN GUIDE, MALE	12
1	1-332056-0	FERRULE	11
6	328666	FERRULE, ORANGE	10
11	201578-1	CONTACT, PIN TYPE II	9
11	201580-1	CONTACT, SOCKET, TYPE II	8
3	201144-1	CONTACT, SOCKET COAX	7
3	201143-1	CONTACT, PIN COAXIAL	6
1	51561-1	CONTACT, PIN, SUBMIN, COAX; AMP	5
6 FT	111707	CABLE, SHIELDED, 16 COND	4
2	9779-513-8 (AN3420-8)	BOOT, CABLE; AMPHENOL	3
1	201598-1	BLOCK, FEMALE HOUSING; AMP	2
1	201597-1	BLOCK, MALE HOUSING; AMP	1

LIST OF MATERIALS

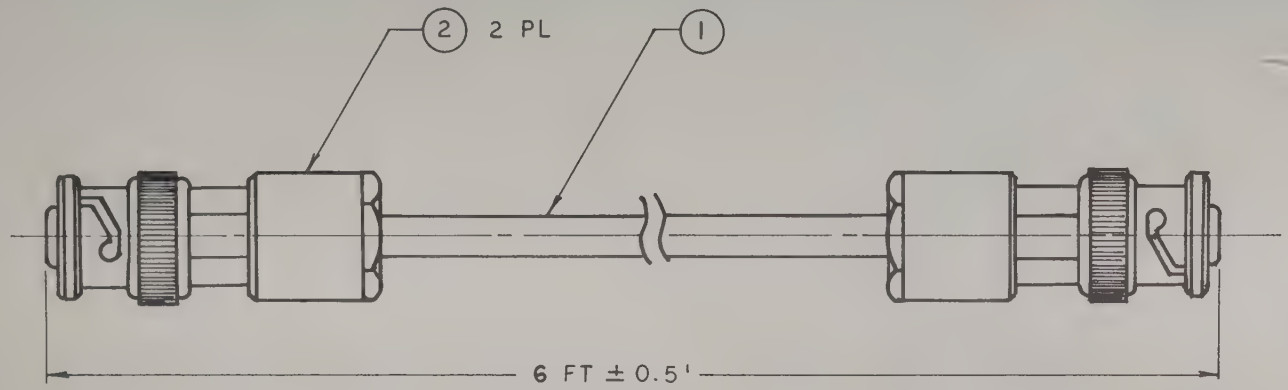
MATERIAL
FINISH
DRAWN MIKLOS
CHECKED
APPROVED [signature]
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± FRAC ±
2 PL DEC ± ANGLES ±

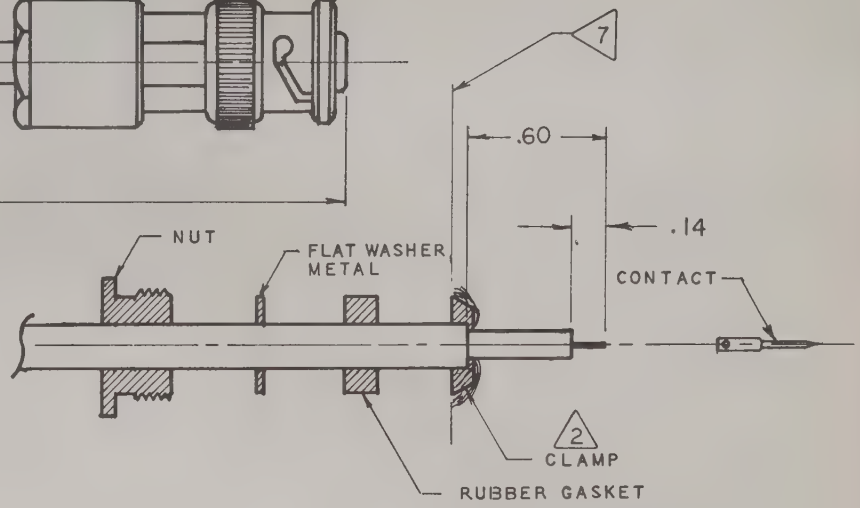
Princeton Applied Research Corporation
Princeton, New Jersey

TITLE
SIGNAL/POWER CABLE, 1205K (SERIES)

SCALE FULL DWG NO. 110398 C
DATE 5-29-74

LETTER	REVISION	DATE	DRWN	CHKD	APR.
A	REDRAWN WITH CHANGES	1-9-72	tvg		





7 BRAID MUST NOT EXTEND BEYOND THIS POINT.

6. INSERT CABLE AND HARDWARE INTO CONNECTOR BODY. SLIDE HARDWARE INTO PLACE AND START NUT. TIGHTEN WITH WRENCH.

5. SOLDER CONTACT ON INNER CONDUCTOR. REMOVE EXCESS SOLDER. DO NOT OVERHEAT DIELECTRIC AS IT WILL BECOME SWOLLEN AND WILL NOT ENTER BODY OR INSULATOR PROPERLY.

4. FLARE BACK BRAID AND TRIM IF NECESSARY. CUT DIELECTRIC TO DIM SHOWN. DO NOT NICK INNER CONDUCTOR.

3. TAPER BRAID, SLIDE NUT WASHER GASKET AND CLAMP (NUT AND NON-SEALING CLAMP) OVER TAPERED BRAID MAKING SURE INNER SHOULDER OF CLAMP IS POSITIONED TIGHTLY AGAINST END OF JACKET.

2 FLARE BRAID BACK OVER CLAMP.

1. CUT OFF END OF CABLE SQUARE AND REMOVE JACKET FROM END AS SHOWN. DO NOT NICK BRAID.

NOTES: EXCEPT AS NOTED

PT. NO. 6020-0320-14

APPROVED FOR PROCUREMENT JH 5-1-75

REQD	PART NO.	DESCRIPTION	ITEM
2	2085-1	CONNECTOR, MHV; DAGE	2
1	RG55B/U	CABLE, COAXIAL	1

LIST OF MATERIALS

MATERIAL:

FINISH:

DRAWN tvg 1-9-72

CHECKED

APPROVED E. Mikuszeski

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

PRINCETON APPLIED RESEARCH

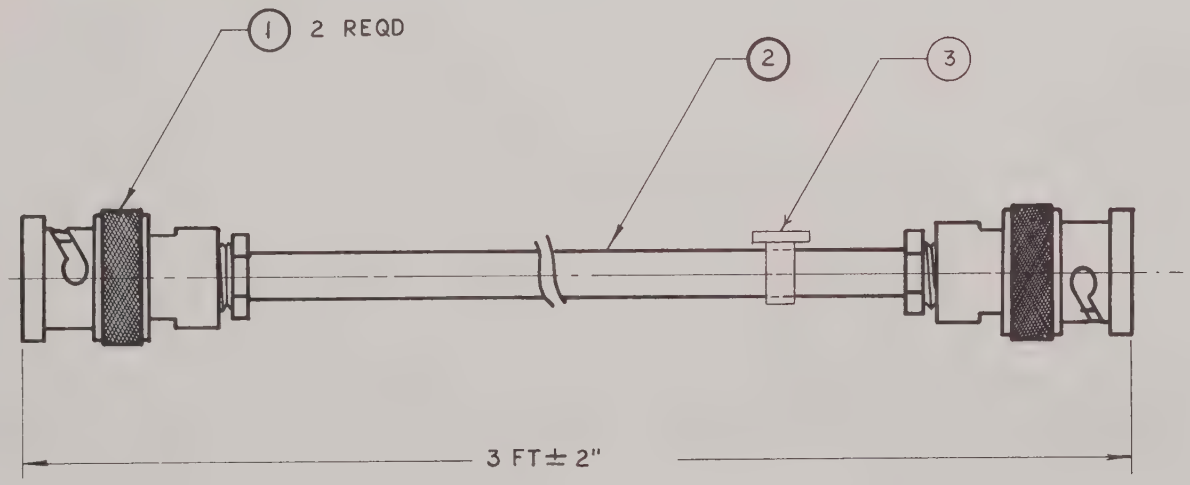
TITLE

HV-CABLE ASSEMBLY

SCALE 2:1 | DWG NO. 110320 B-ESA | A

DATE 1-9-72

LETTER	REVISION	DATE	DRWN	CHKD	APR.



NOTE:
THIS ITEM MAY BE PURCHASED WITH CRIMP-TYPE CONNECTORS SUBJECT TO R&D APPROVAL OF SAMPLES.

APPROVED FOR PROCUREMENT 4-11-75

REQD	PART NO.	DESCRIPTION	ITEM
1	PLMIM-M	LABEL, PANDUIT (2802-0058-07)	3
3'	RG-55B/U	CABLE, COAXIAL (6005-0014-06)	2
2	UG-88C/U	CONNECTOR, BNC (2102-0119-01)	1

LIST OF MATERIALS

MATERIAL:
FINISH:
DRAWN MICLOG
CHECKED
APPROVED CAS 4-29-75
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± | FRAC ±
2 PL DEC ± | ANGLES ±

PRINCETON APPLIED RESEARCH

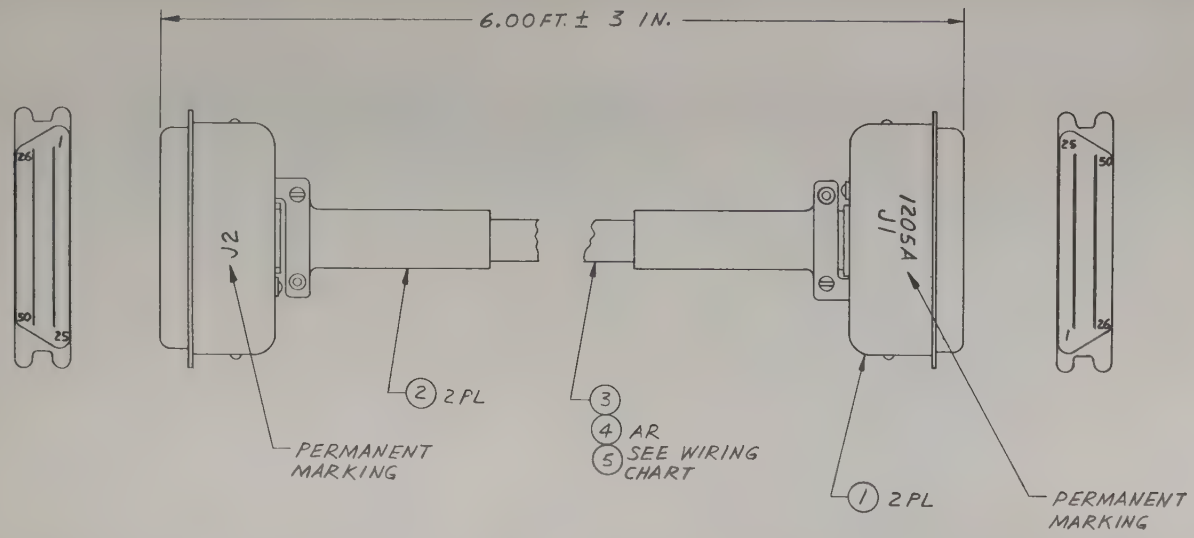
TITLE
CABLE, BNC, INPUT-

SCALE 2 : 1
DATE 12-29-74
DWG NO. 110322 -B- ESA

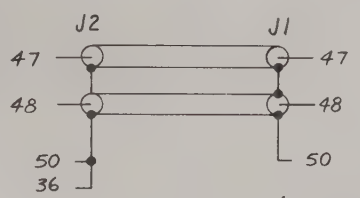
PT. NO. 6020-0322-04

NOTES: EXCEPT AS NOTED

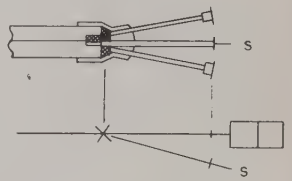
LETTER	REVISION	DATE	DRWN	CHKD	APR



NOTE :
ATTACH TAG (RA.R.C. 2802-0058-07)
PANDUIT PLMIM WITH P.A.R.C.
PART NO 6020-0375-05



DETAIL - A
SHIELDS TIE TO PIN 50



DETAIL - H

WIRING CHART

FROM	TO	COLOR CODE
J1 - 1	J2 - 1	BROWN
- 2	- 2	RED
- 3	- 3	ORANGE
- 4	- 4	YELLOW
- 5	- 5	GREEN
- 6	- 6	BLUE
- 7	- 7	VIOLET
- 8	- 8	GREY
- 9	- 9	WHITE
- 10	- 10	WHITE / BLACK
- 11	- 11	WHITE / BROWN
- 12	- 12	NO WIRE (SPARE)
- 13	- 13	WHITE / ORANGE
- 14	- 14	WHITE / YELLOW
- 15	- 15	WHITE / GREEN
- 16	- 16	WHITE / BLUE
- 17	- 17	WHITE / VIOLET
- 18	- 18	WHITE / GREY
- 19	- 19	SL. / WHITE
- 20	- 20	GREEN / BLACK
- 21	- 21	GREEN / BROWN
- 22	- 22	NO WIRE (SPARE)
- 23	- 23	NO WIRE (SPARE)
- 24	- 24	NO WIRE (SPARE)
J1 - 25	J2 - 25	SL. / GREEN

FROM	TO	COLOR CODE	
J1 - 26	J2 - 26	GREEN / BLUE	
- 27	- 27	GREEN / VIOLET	
- 28	- 28	GREEN / GREY	
- 29	- 29	GREEN / WHITE	
- 30	- 30	ORANGE / BLACK	
- 31	- 31	ORANGE / BROWN	
- 32	- 32	ORANGE / RED	
- 33	- 33	SL. / RED	
- 34	- 34	ORANGE / YELLOW	
- 35	- 35	ORANGE / GREEN	
- 36	- 36	NO WIRE	
- 37	- 37	NO WIRE (SPARE)	
- 38	- 38	ORANGE / GREY	
- 39	- 39	NO WIRE (SPARE)	
- 40	- 40	YELLOW / BLACK	
- 41	- 41	YELLOW / BROWN	
- 42	- 42	YELLOW / RED	
- 43	- 43	YELLOW / ORANGE	
- 44	- 44	SL. / YELLOW	
- 45	- 45	YELLOW / GREEN	
- 46	- 46	NO WIRE (SPARE)	
- 47	- 47	COAX	SEE DETAIL A & H
- 48	- 48	COAX	SEE DETAIL A & H
- 49	- 49	NO WIRE (SPARE)	
J1 - 50	J2 - 50	SHIELD	SEE DETAIL A & H
NC	NC	SL. / BROWN (SPARE)	
NC	NC	SL. / BLUE (SPARE)	
J2 - 36	J2 - 50	SL / BLACK	SEE DETAIL A & H

APPROVED FOR PROCUREMENT DCN 6/15

REQD	PART NO.	DESCRIPTION	ITEM
AR	RG174	SHIELDED CABLE, COAX	5
AR	MIL-W-16878D	WIRE, INS., TYPE BU, 24 AWG	4
1	PVC105-1/2	TUBING, PVC 1/2ID ALPHA	3
2	9779-513-10	BOOT, AN3470 AMPHENOL	2
2	57-30500	CONNECTOR, 50 PINS, AMPHENOL	1

LIST OF MATERIALS

MATERIAL:
FINISH:
DRAWN Dyer
CHECKED
APPROVED M. Mitsukoshi
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± | FRAC ±
2 PL DEC ± | ANGLES ±

PRINCETON APPLIED RESEARCH

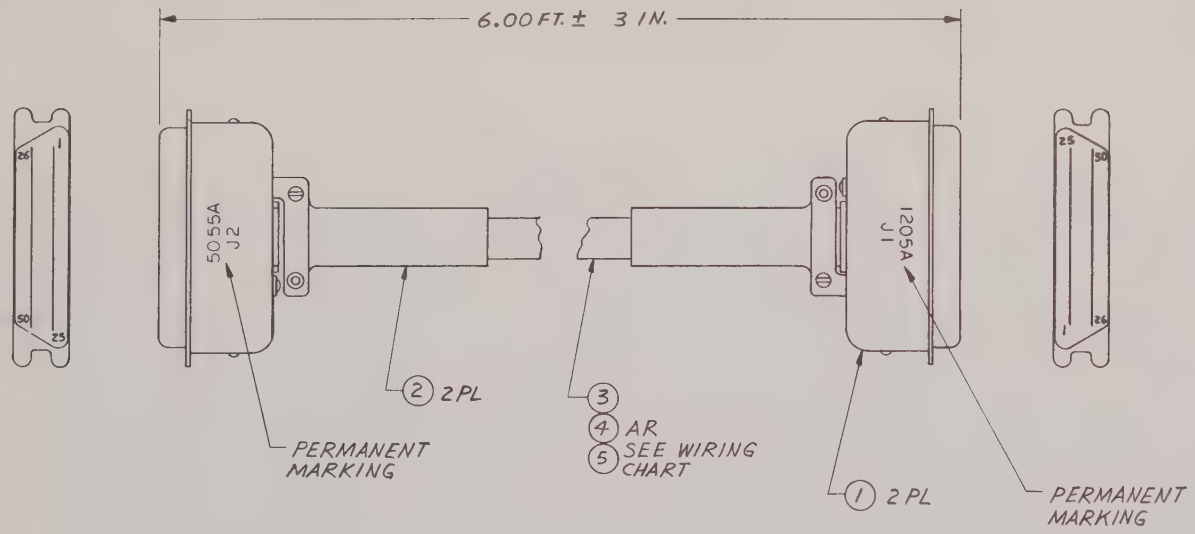
TITLE
PRINTER- CABLE
1205A TO 1110 PRINTER

SCALE NONE
DATE
DWG NO. 110375-C-ESA

XII-45

LETTER	REVISION	DATE	DRWN	CHKD	APR.

X1146

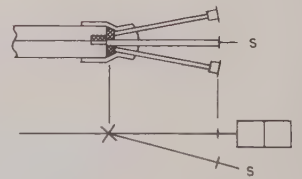


NOTE :
ATTACH TAG (P.A.R.C. 2807-0058-07)
PANDUIT PLMIM WITH P.A.R.C.
PART NO 6020-0380-03

WIRING CHART

FROM	TO	COLOR CODE	FROM	TO	COLOR CODE	
J1 - 1	J2 - 1	BROWN	J1 - 26	J2 - 26	GREEN / BLUE	
- 2	- 2	RED	- 27	- 27	GREEN / VIOLET	
- 3	- 3	ORANGE	- 28	- 28	GREEN / GREY	
- 4	- 4	YELLOW	- 29	- 29	GREEN / WHITE	
- 5	- 5	GREEN	- 30	- 30	ORANGE / BLACK	
- 6	- 6	BLUE	- 31	- 31	ORANGE / BROWN	
- 7	- 7	VIOLET	- 32	- 32	ORANGE / RED	
- 8	- 8	GREY	- 33	- 33	SL. / RED	
- 9	- 9	WHITE	- 34	- 34	ORANGE / YELLOW	
- 10	- 10	WHITE / BLACK	- 35	- 35	ORANGE / GREEN	
- 11	- 11	WHITE / BROWN	- 36	- 36	ORANGE / BLUE	
- 12	- 12	WHITE / RED	- 37	- 37	NO WIRE (SPARE)	
- 13	- 13	WHITE / ORANGE	- 38	- 38	ORANGE / GREY	
- 14	- 14	WHITE / YELLOW	- 39	- 39	NO WIRE (SPARE)	
- 15	- 15	WHITE / GREEN	- 40	- 40	YELLOW / BLACK	
- 16	- 16	WHITE / BLUE	- 41	- 41	YELLOW / BROWN	
- 17	- 17	WHITE / VIOLET	- 42	- 42	YELLOW / RED	
- 18	- 18	WHITE / GREY	- 43	- 43	YELLOW / ORANGE	
- 19	- 19	SL. / WHITE	- 44	- 44	SL. / YELLOW	
- 20	- 20	GREEN / BLACK	- 45	- 45	YELLOW / GREEN	
- 21	- 21	GREEN / BROWN	- 46	- 46	NO WIRE (SPARE)	
- 22	- 22	NO WIRE (SPARE)	- 47	- 47	COAX	SEE DETAIL A & H
- 23	- 23	NO WIRE (SPARE)	- 48	- 48	COAX	SEE DETAIL A & H
- 24	- 24	NO WIRE (SPARE)	- 49	- 49	NO WIRE (SPARE)	
J1 - 25	J2 - 25	SL. / GREEN	J1 - 50	J2 - 50	SHIELD	SEE DETAIL A & H
			NC	NC	SL. / BROWN (SPARE)	
			NC	NC	SL. / BLUE (SPARE)	

DETAIL - A
SHIELDS TIE TO PIN 50



DETAIL - H

APPROVED FOR PROCUREMENT 5-1-75

REQD	PART NO.	DESCRIPTION	ITEM
AR	RG174	SHIELDED CABLE, COAX	5
AR	MIL-W-16878D	WIRE, INS., TYPE BU, 24 AWG	4
1	PVC105-1/2	TUBING, PVC 1/2ID ALPHA	3
2	9779-513-10	BOOT, AN3420, AMPHENOL	2
2	57-30500	CONNECTOR, 50 PINS, AMPHENOL	1

LIST OF MATERIALS

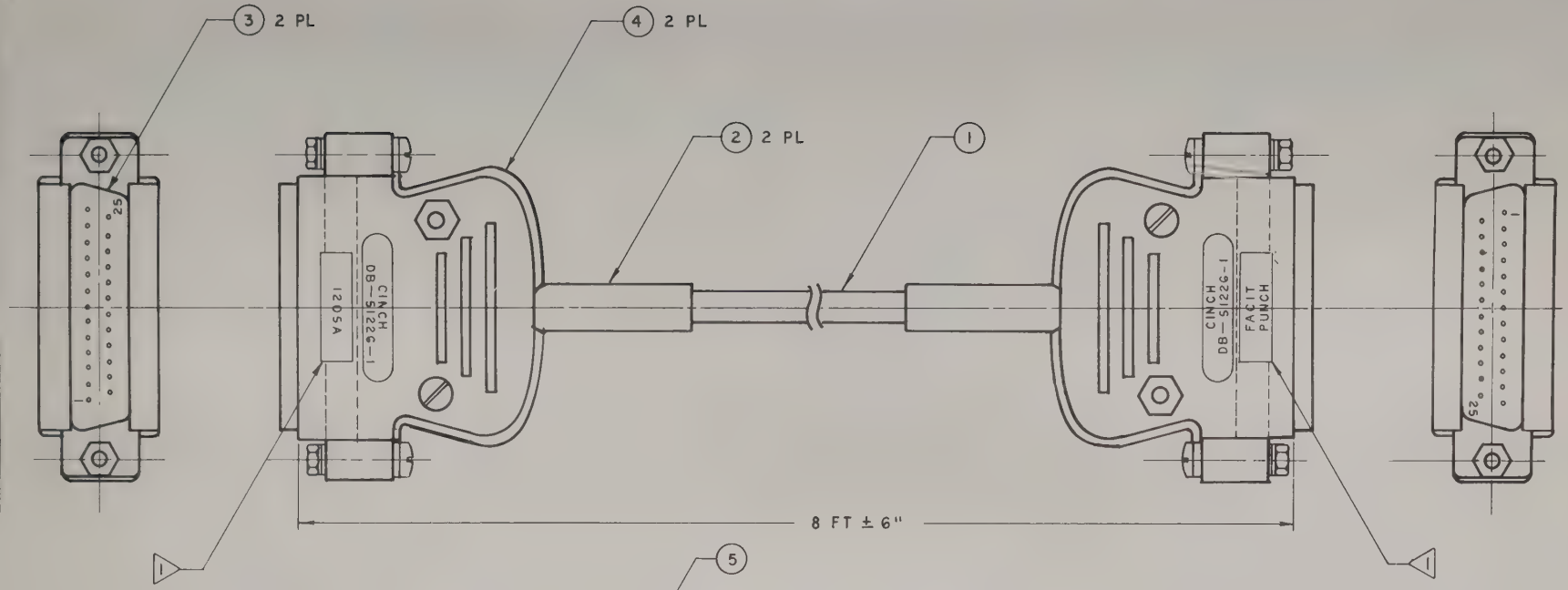
MATERIAL:
FINISH:
DRAWN
CHECKED
APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
3 PL DEC ± | FRAC ±
2 PL DEC ± | ANGLES ±

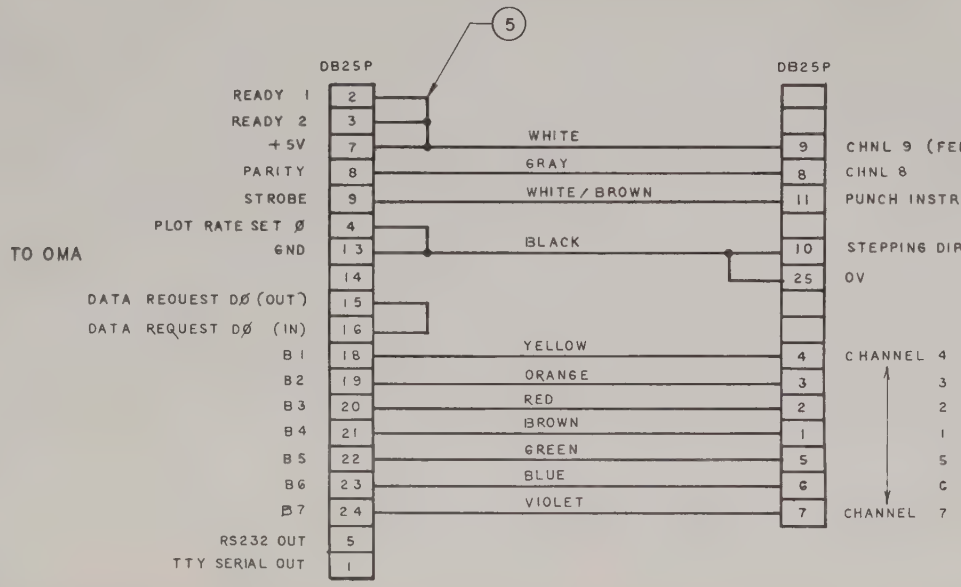
PRINCETON APPLIED RESEARCH

TITLE
PRINTER - CABLE
1205A TO 5055A

SCALE NONE
DWG NO. 110380-C-ESA
DATE

LETTER	REVISION	DATE	DRWN	CHKD	APR





APPROVED FOR PROCUREMENT:

TO FACIT PUNCH

PT. NO. 6020-0383-00

REQD	PART NO.	DESCRIPTION	ITEM
24"	# 22 GA	WIRE, BUSS	5
2	DB51226-1	SHELL, CONN; CINCH	4
2	DB25P	CONNECTOR, CINCH	3
2	9779-513-4	BOOT, CABLE; AMPHENOL	2
108"	6003-0010-02	CABLE, 15 CONDUCTOR	1

LIST OF MATERIALS

MATERIAL

FINISH

DRAWN MIKLOS

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

PRINCETON APPLIED RESEARCH

TITLE

CABLE ASSEMBLY, 1205A TO FACIT PUNCH-CHAR. SERIAL

SCALE 2:1 | DWG NO. 10383-C-ESA

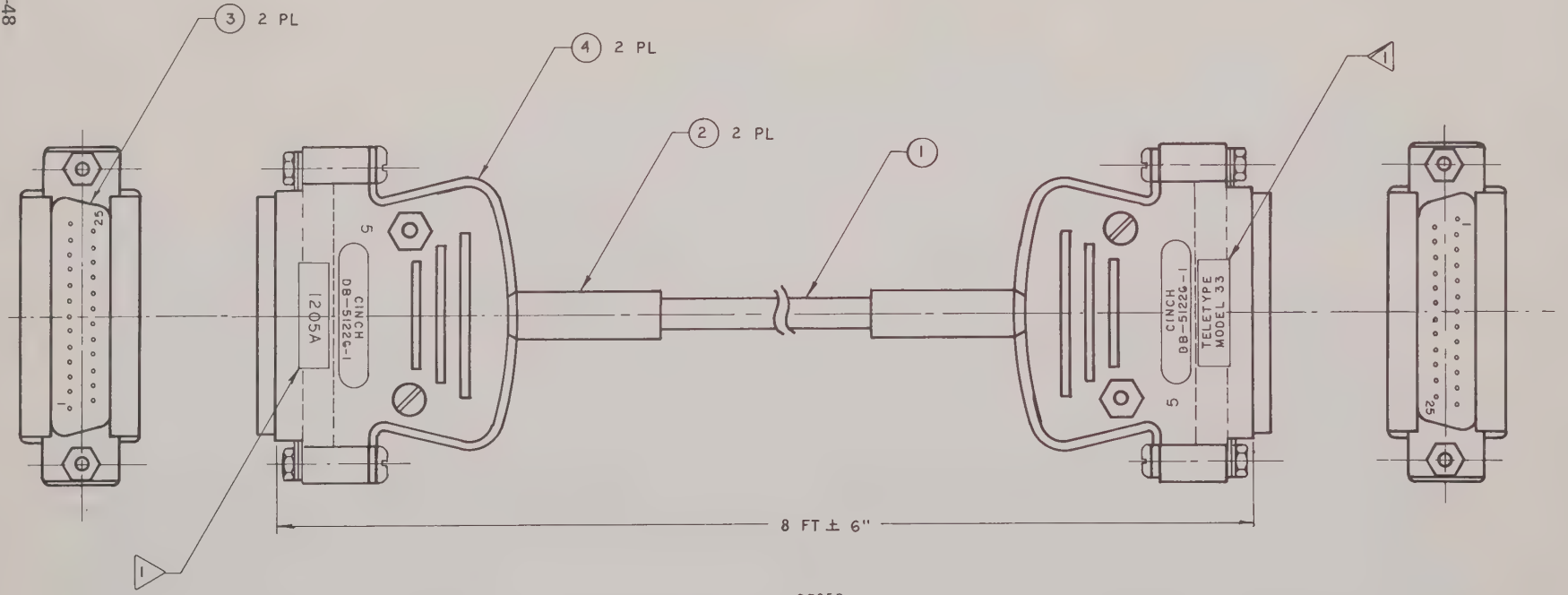
DATE 11-2-73

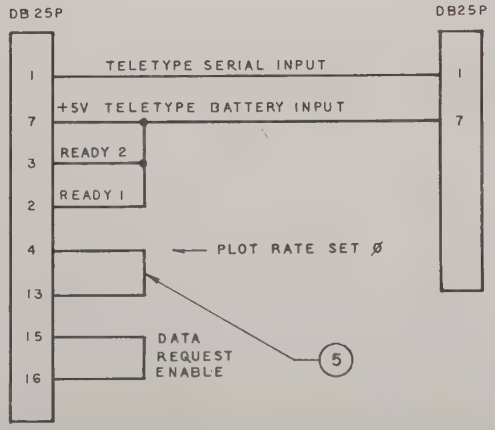
XII-47

⚠1 PERMANENT MARK AS SHOWN.

NOTES: EXCEPT AS NOTED

LETTER	REVISION	DATE	DRWN	CHKD	APR





TO OMA 1205A

TO TELETYPE MODEL 33

APPROVED FOR PROCUREMENT

REQD	PART NO	DESCRIPTION	ITEM
A/R	#22 GA	WIRE, BUSS	5
2	DB56226-1	SHELL, CONN.; CINCH	4
2	DB25P	CONNECTOR; CINCH	3
2	9779-513-4	BOOT, CABLE; AMPHENOL	2
1	8737	CABLE, 2COND, 22 AWG; BELDEN	1

LIST OF MATERIALS

MATERIAL

FINISH

DRAWN MIKLOS

CHECKED

APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± | FRAC ±

2 PL DEC ± | ANGLES ±

TITLE

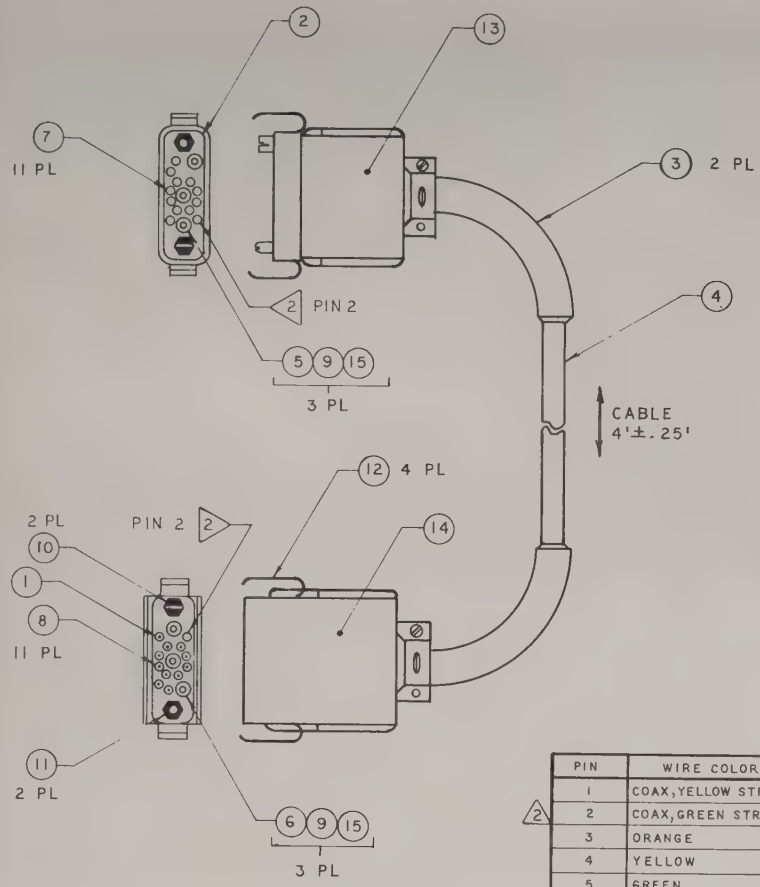
CABLE ASSEMBLY 1205A TO TELETYPE MODEL 33

SCALE 2:1 | DWG NO. 110382 C

DATE 9-10-73 | ESA

1 PERMANENT MARK AS SHOWN.

NOTES EXCEPT AS NOTED.



PIN	WIRE COLOR	FUNCTION
1	COAX, YELLOW STRIPE	FRRETRACEDØ
2	COAX, GREEN STRIPE	
3	ORANGE	OMA+5V SUPPLY
4	YELLOW	OMA-15V SUPPLY
5	GREEN	GROUND
6	BLUE	AACCUMSWDØ
7	COAX, WHITE STRIPE	NOT USED
8	GRAY	BACCUMSWDØ
9	WHITE	DELINHDI
10	BLACK-WHITE	DELBLANK2DØ
11	BROWN-WHITE	PRECLOCK2DØ
12	RED	FILONA-
13	COAX, PLAIN	VCATHAN
14	BROWN	SDELAYDØ
15	VIOLET	REALSWDØ
SHELL	BRAIDED SHIELD	

2 NO PIN CONNECTED OR INSTALLED.

1. MALE GUIDE PIN.
   FEMALE GUIDE PIN.

NOTES: EXCEPT AS NOTED.

LETTER	REVISION	DATE	DRWN	CHKD	APR
A	ITEM 7 WAS 201328-1 & ITEM 9 WAS 201330-1. DLN 3206	1-7-73	FB	[illegible]	[illegible]

PT. NO. 6020-0390-19

APPROVED FOR PROCUREMENT _____

			20
			19
			18
			17
			16
6	201142-2	SPRING, RETENTION, AMP	15
1	201382-2	SHIELD, 180° PIN PROTECTION;	14
1	201169-2	SHIELD, 180° NON PROTECTED;	13
2	201923-1	SET, LOCKING SPRING;	12
2	200390-4	PIN GUIDE, FEMALE,	11
2	200389-4	PIN GUIDE, MALE;	10
6	328666	FERRULE, ORANGE;	9
11	201578-1	CONTACT, PIN TYPE II;	8
11	201580-1	CONTACT, SOCKET, TYPE II; AMP	7
3	201144-1	CONTACT, SOCKET COAXICON	6
3	201143-1	CONTACT, PIN, COAXICON	5
4'	111707	CABLE, SHIELDED, 16 COND; ANY	4
2	9779-513-8 (AN3420-8)	BOOT CABLE; AMPHENOL	3
1	201598-1	BLOCK, FEMALE HOUSING; AMP	2
1	201597-1	BLOCK, MALE HOUSING; AMP	1
REQD	PART NO	DESCRIPTION	ITEM

LIST OF MATERIALS

MATERIAL

FINISH

DRAWN

CHECKED

APPROVED B. Matsuhashi

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

3 PL DEC ± FRAC ±

2 PL DEC ± ANGLES ±

PRINCETON APPLIED RESEARCH

TITLE

CABLE, INTERFACE - 1205A TO 1207

SCALE 2 : 1 DWG NO 110390 A

DATE 3-8-73

XII-49

NOTES

MP MASTER
MA28897

PRINCETON APPLIED RESEARCH

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